10-Gbps BURST MODE CR AND OPTICAL PACKET TRANSCEIVER —50-ps LOCK-IN CLOCK RECOVERY AND ITS APPLICATION—

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We have developed a high-speed burst mode clock recovery (Burst CR) IC operating on a lock-in time of 50 ps, i.e. a half bit of 10-Gbps data, and have developed an optical packet transceiver which incorporates the Burst CR. These are based on indispensable technologies for accurate communications and stable operations in next-generation optical networks such as optical packet networks and 10G-PON (Passive Optical Network), and will greatly contribute to earlier implementation of such optical networks.

INTRODUCTION

With the spread of broadband Internet connections in recent years, large volumes of data such as video are being transmitted. To carry this sharp rise in traffic, networks need to be made faster.

Broadcast stations are also considering introducing high-speed networks because they need to handle large volumes of data as well as digital data. In high-performance computing (HPC), high-speed networks are required for communications among high-performance nodes. Optical packet networks offer a promising solution to meet these needs; although research is still underway, such networks will switch optical signals without optical-electrical conversion at relay node routers, offering various advantages in scalability and latency.

Packet communications transmit/receive data divided into small units, or packets. Each packet is discontinuous and asynchronous burst data. For stable communications, it is important to recover a clock signal from burst data. The lock-in time, which is the time from receiving burst data to synchronizing a clock signal with the data, is wasted time because effective communications cannot be carried out during this period. Therefore, a shorter lock-in time is desirable in next-generation optical communications networks.

The newly developed burst mode clock recovery IC (“Burst CR”) described in this paper can be applied to 10-Gbps high-speed communications. The lock-in time is 50 ps, which is equivalent to a half bit of data. The IC has superior transmission efficiency for high-speed communications. We have also developed an optical packet transceiver, which includes the Burst CR and has several functions necessary for developing next-generation optical communications networks such as transmitting/receiving burst data or connection to an upper system through a low-speed side electrical interface compliant with the 300-pin Multi-Source Agreement Standard (MSA).

THE NEED FOR OPTICAL PACKET COMMUNICATIONS

Packet communications are widely used in local area networks (LAN) and the Internet. In this system, multiple nodes can share a single line, which means that no line is occupied by point-to-point communications. Therefore, it is an economical communications system with high efficiency of line usage, and nodes can be flexibly extended.

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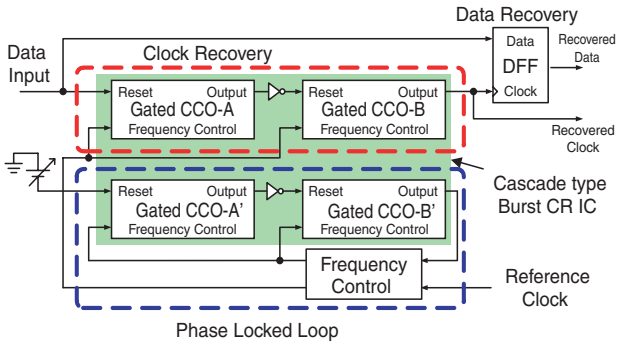

Figure 1 Configuration of Cascade Type Burst CR

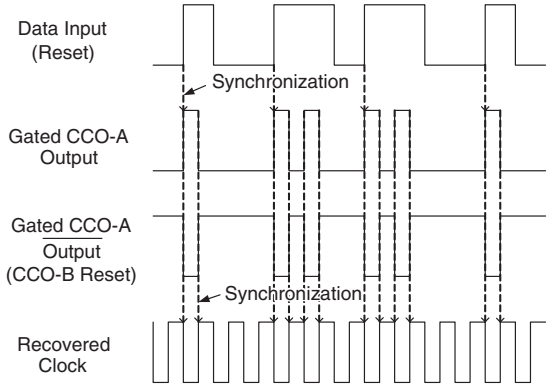

Figure 2 Timing Chart of Cascade Type Burst CR

Currently, electrical communications through metal cables is the mainstream in view of cost. For high-speed communications at over 10 Gbps, optical transmission is desirable to solve the issues of reach and so forth. However, optical-electrical conversion at nodes or routers increases the latency and power consumption.

Optical packet networks will solve this problem: the networks switch optical signals as packets, so there is no need for optical-electrical conversion, thus reducing both the latency and power consumption.

Optical packet networks will be used in next-generation HPC communications among nodes or intra-communications in broadcast stations. In a Passive Optical Network (PON), which connects households with a telecommunications branch to provide Internet connectivity, communication is carried out using optical packets. The PON system divides a single fiber by using optical couplers and sends the optical signals to multiple households or subscribers. Upload data is divided into packets, which are then transmitted to the telecommunications branch separately. The branch needs to receive asynchronous burst data because transmission among each household and the telecommunications branch is asynchronous.

To deal with surges in traffic, PON in the 10-Gbps band (10 G-PON) is being researched, but the technology for receiving burst data remains a challenge. To solve the problem, low power consumption, stable operation, and a high-speed lock-in time of clock recovery are needed. Our Burst CR and packet transceiver will help address these needs.

BURST CR

Advantages of Burst CR

We have developed a cascade type Burst CR which recovers clock information by using two serially-connected oscillators. In this design, all the circuits operate as differential circuits, and have low dependency on temperature or power source. High-speed lock-in is achieved by resetting each oscillator at rising edges and down edges of input data. This Burst CR has smaller circuits and lower power consumption than conventional technologies.

Configuration of Burst CR

Figure 1 shows a block diagram of the cascade type Burst CR. The oscillators indicated as Gated CCOs (current-controlled oscillators) are a ring oscillator comprised of a differential inverter. The AND circuit in the ring oscillator acts as a resetting function and is activated when “Low” is input and the oscillator stops oscillating. The output of the previous oscillator (CCO-A) is inversely connected to the reset input of the next oscillator (CCO-B). The output of CCO-B is used for recovering clock information. The recovery clock operates the Delay Flip-Flop (DFF) in which data is recovered.

At each oscillator, current is kept constant by a current mirror circuit. The oscillating frequency is controlled by adjusting the current. Adjacent to the oscillators (CCO-A/CCO-B), oscillators with the same characteristics (CCO-A’/CCO-B’) are placed to serve as a Phase Locked Loop (PLL). These help to maintain the oscillating frequency even when the conditions such as the power source or temperature change.

Principle of operation

Figure 2 shows the timing chart of the cascade type Burst CR.

The change of input data to “High” switches the reset input and output of CCO-A to “High.” At the same time, the reset input of CCO-B changes to “Low” and stops oscillation because the output of CCO-A is inversely connected.

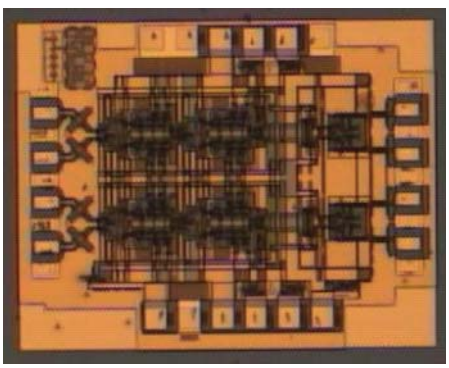

Figure 3 Photograph of Chip in Cascade Type Burst CR

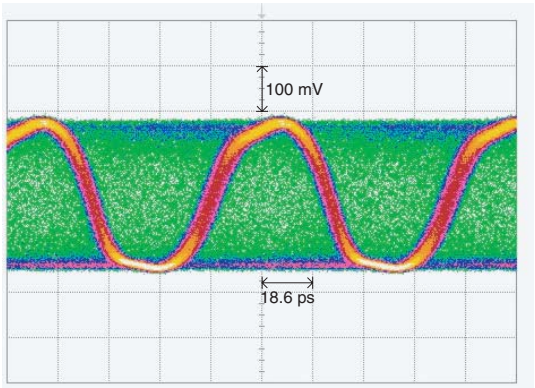

Figure 4 Waveform of Recovery Clock upon Receiving Burst Data

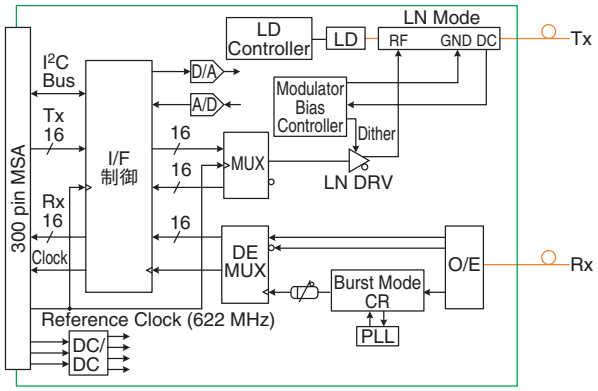

Figure 6 Configuration of Optical Packet Transceiver

While input is maintained "High," CCO-A and CCO-B oscillate in synchronization except that the CCO-B outputs the opposite value because it is inversely connected with the output of CCO-A.

When the input data changes to "Low," CCO-A stops oscillating and outputs "Low," which changes the reset input of CCO-B to "High" and CCO-B outputs the clock.

As described above, the system can continuously recover clock information synchronized with input data, and can promptly output the clock synchronized with input data even when it is burst data.

Evaluation of developed Burst CR and its specifications

Figure 3 shows a photograph of the chip in the cascade type Burst CR. The chip specifications are dimensions of 2 mm × 1.6 mm, power voltage of –3.3 V, and power consumption of about 1.2 W. The compound semiconductor material is InP, the process rule is 2 μm, and a hetero-bipolar transistor is used for the semiconductor device[1].

Figure 4 shows the recovery clock when the bit rate of input data is 11.5 Gbps, length of pseudo-random bit sequence (PRBS) is 2^{15}–1, data length is 2.5 μs, and gap length (non-signal interval of burst data) is 348 ns. There is a green part looks like a belt behind the waveform of the recovery clock. This is because the recovery clock becomes a free-run clock during the gap with no data and does not synchronize with the trigger of the oscilloscope. Figure 5 shows the recovery clock at the head of the pattern. The recovery clock is locked in at 50 ps, which is equivalent to a half bit of data at the head of packet data. This 50 ps is a sufficiently short time even considering switching time, therefore the system can make full use of the bandwidth in networks.

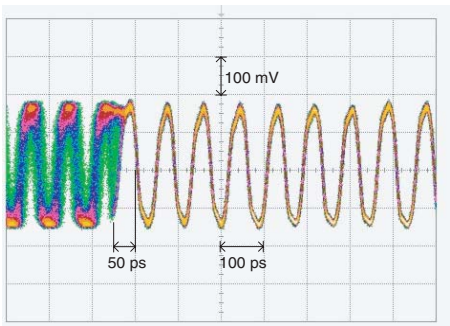

Figure 5 Waveform of Recovery Clock upon Receiving Burst Data (At the Head of Data)

OPTICAL PACKET TRANSCEIVER

Advantages of optical packet transceiver

We have developed an optical packet transceiver equipped with the cascade type Burst CR IC. The transceiver has an advantage of high-speed lock-in requiring no signals added to the head of packet data ("preamble") which synchronize received data to clock information and has high transmission efficiency. By integrating the Burst CR and O/E conversion part in a ceramic module, the size is reduced. The transmitting part uses DC current to output burst data with long gaps. The transceiver is connected with an upper system through a 300-pin MSA connector and its electrical interface is compliant with the Optical Internetworking Forum (OIF) SFI-4 standards. Digital to Analog Converter (DAC) control information or internal information can also be transmitted to the upper system through the I^2C bus.

Configuration of optical packet transceiver

Figure 6 shows the configuration of the optical packet transceiver.

The receiving part is comprised of the O/E converting part, Burst CR, and DEMUX (de-multiplexer). The O/E converting part converts received optical signals into electrical signals and the Burst CR recovers clock information from the signals. DEMUX carries out data recovery and de-multiplexes the data by using the recovered clock information.

The transmitting part is comprised of a MUX (multiplexer), LN (Lithium Niobate) DC driver, and LN modulator. The data multiplexed at MUX is output from the electric/optical converting part consisting of the LN DC driver and the LN modulator.

In addition, the 300-pin MSA connector, I/F control circuit, and circuit controlling the internal information via the I^2C bus are

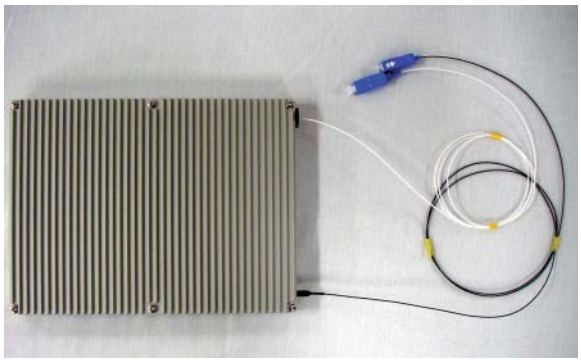

Figure 7 Photograph of Optical Packet Transceiver

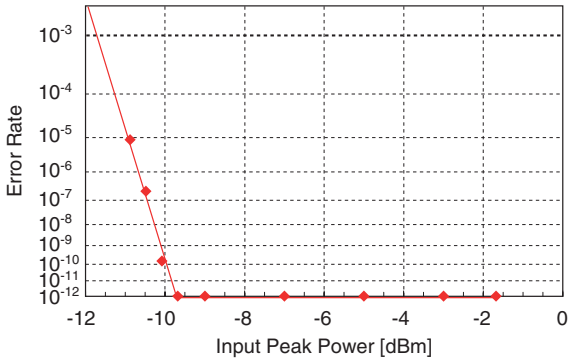

Figure 9 BER Characteristics of Optical Packet Transceiver

implemented.

Evaluation of developed optical packet transceiver and its specifications

Figure 7 shows a photograph of the optical packet transceiver. Its dimensions are 200 × 150 × 19 mm.

The evaluation tests were conducted by using the electric loop-back method. The optical signals are received at the receiving part of the optical packet transceiver, output as optical signals from the transmitting part, converted into electrical signals, and measured for error rates or quality of waveform.

Figure 8 shows waveforms under the following conditions: ambient temperature of 25°C, input signal bit rate of 10.72 Gbps, RBS length of 2^{15}–1, data length of 3 μs, gap length of 18.7 ns, and input power of –4 dBm. The results revealed that jitter is 3.6 ps (RMS) and extinction ratio is 11.3 dB. The Bit Error Rate (BER) characteristic is shown in Figure 9; a dynamic range of 8.0 dB was obtained.

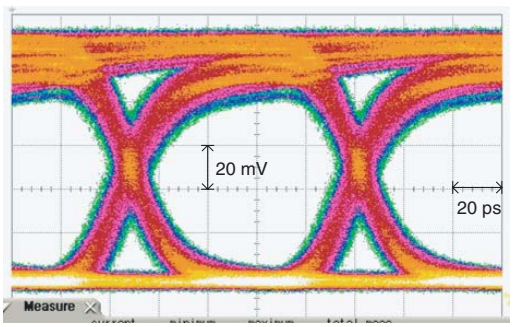

Figure 8 Output Waveform of Optical Packet Transceiver (Electric loop-back)

In systems such as optical packet networks that transmit/receive burst data with long gaps, the frequency elements of data tend to extend to extremely low bands because the data gaps are DC components. Therefore, the signal lines need to be configured based on DC connection. Adding preamble to every packet to control the gain or offset of amplifiers is not desirable for transmission efficiency. This makes it technically difficult to achieve a sufficient dynamic range. Our system, however, achieves a wide dynamic range of 8.0 dB by incorporating photodiodes with high sensitivity and Burst CR with differential input.

CONCLUSION

We have developed a Burst CR with the advantages of clock recovery from high bit rate burst data and high-speed lock-in, and have also developed an optical packet transceiver equipped with the Burst CR. This transceiver, which is compact and has low power consumption, saves energy and reduces operating costs. It will be useful for next-generation optical communications in the short- to medium-range such as next-generation PON, node-to-node communications among supercomputers, and intra-networks in broadcast stations and companies.

We are planning to develop 40-Gbps equipment and to downsize the optical packet transceiver. ◆

REFERENCE

(1) MIURA Akira, MATSUURA Hiroyuki, WADA Morio, YAKIHARA Tsuyoshi, KODAKA Hirotoshi, IKEZAWA Katusya, "Photonic Measurement and Control Technologies," Yokogawa Technical Report, No. 41, 2006, pp. 33-44

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