DL9700/DL9500 SERIES OF DIGITAL MIXED SIGNAL OSCILLOSCOPE

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We have developed the DL9700/DL9500 series of mixed signal oscilloscope, featuring 32-bit maximum logic input, a 250-MHz maximum logic input toggle frequency, a maximum analog frequency bandwidth of 1.0 GHz, a maximum sampling rate of 5 GS/s and a maximum recording length of 6.25 M word. This series is characterized by high-performance functions of waveform display and analysis with a high sampling rate and long memory in both analog/logic inputs, thus providing the best environment for analog/logic signal harmonized analysis of embedded systems.

INTRODUCTION

Yokogawa has already been offering the DL7400 series of mixed signal oscilloscopes, featuring 500 MHz analog frequency bandwidth, 16-bit logic input, and 2 GS/s maximum sample rate. Recently, we have released the DL9700/DL9500 series with 1.0 GHz analog frequency bandwidth, 32-bit maximum logic input, 5 GS/s maximum sampling rate in both analog/logic inputs, and 6.25 M word maximum recording length to realize outstanding waveform display and analysis functions. Figure 1 shows the external view of this oscilloscope.

The DL9700/DL9500 series achieves compact size of about 28% reduced volume and about 26% reduced weight compared to DL7480 by the integration of signal processors and low power consumption design. It also boasts low noise with the optimization of internal heat release paths and airflow.

Table 1 shows the specifications of each model of the DL9700/DL9500 series. Four models are available for different analog frequency bandwidths and the number of logic inputs. The 32-bit logic input model comes with data bus and address bus, as well as adequate inputs for the simultaneous observation of control signals for clock and chip select and signals of peripheral circuits. These diverse trigger and analysis functions enhance the functions of this new series of mixed signal oscilloscopes.

This report describes product configurations, as well as the logic input signal processor and distinctive functions of the DL9700/DL9500 series.

CONFIGURATION

Figure 2 shows the circuit configuration of the DL9700/

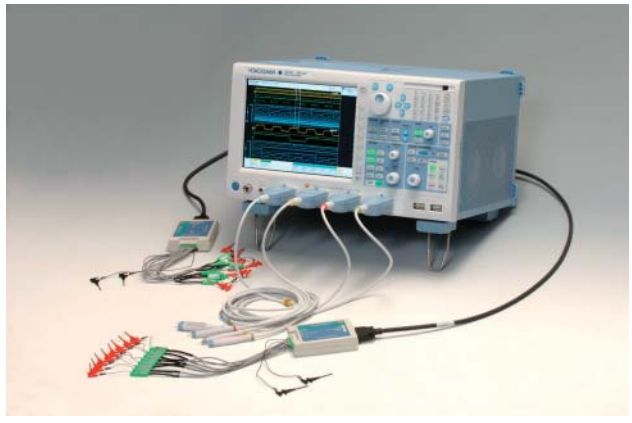

Figure 1 External View of DL9700/DL9500 Series

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Table 1 Specifications of Each DL9700/DL9500 Model

Model name	DL9710L	DL9705L	DL9510L	DL9505L
Analog input channels	4 CH			
Bandwidth	1 GHz	500 MHz	1 GHz	500 MHz
Number of logic inputs	32 bit		16 bit	
Max, toggle frequency*2	250 MHz			
Max, sampling rate	5 GS/s			

*2 Maximum frequency which can be acquired for both rising edge and falling edge

DL9500 series.

The analog block is made up of the same circuit configuration as the DL9000 series. Using cascade 2.5 GS/s 8-bit A/D converters with low power consumption design, these are operated in parallel to realize the maximum sampling rate of 5 GS/s.

A new logic signal sampler LPS (Logic Probe Sampler) was developed for the logic block to realize the same sampling rate as the 5 GS/s analog block.

The signal processing block has the same configuration as the analog block and logic block, and works to generate display data from data discretized by an A/D converter and LPS, and carry out computation of various waveform parameters. The ADSE (Advanced Data Stream Engine) is a CMOS IC incorporating data memory, whose unique architecture realizes high speed waveform update rate of 25,000 waveforms/sec, which is about 400 times that of the DL7400 series.

Figure 3 shows the configuration of the LPS and Table 2 shows the main specifications.

It has two circuits of the 8-bit, 2.5 GS/s samplers, realizing the maximum sampling rate of 5 GS/s through their parallel operations. Data discretized by these samplers is parallel-output, lowering the data rate to the input bandwidth of the next stage signal processing block ADSE. The input block is equipped with a buffer for branching data to the trigger signal processing circuit.

The LPS sampling clock is multiplied with the system base clock at the PLL circuit and is generated for every LPS. The LPS incorporates the frequency divider, phase frequency comparator, and charge pump circuit required for the PLL circuit, and generates sampling clocks by connecting to an external loop filter and VCO.

The DL9700/DL9500 series have a built-in sampling clock phase adjusting circuit to synchronize the four samplings of the

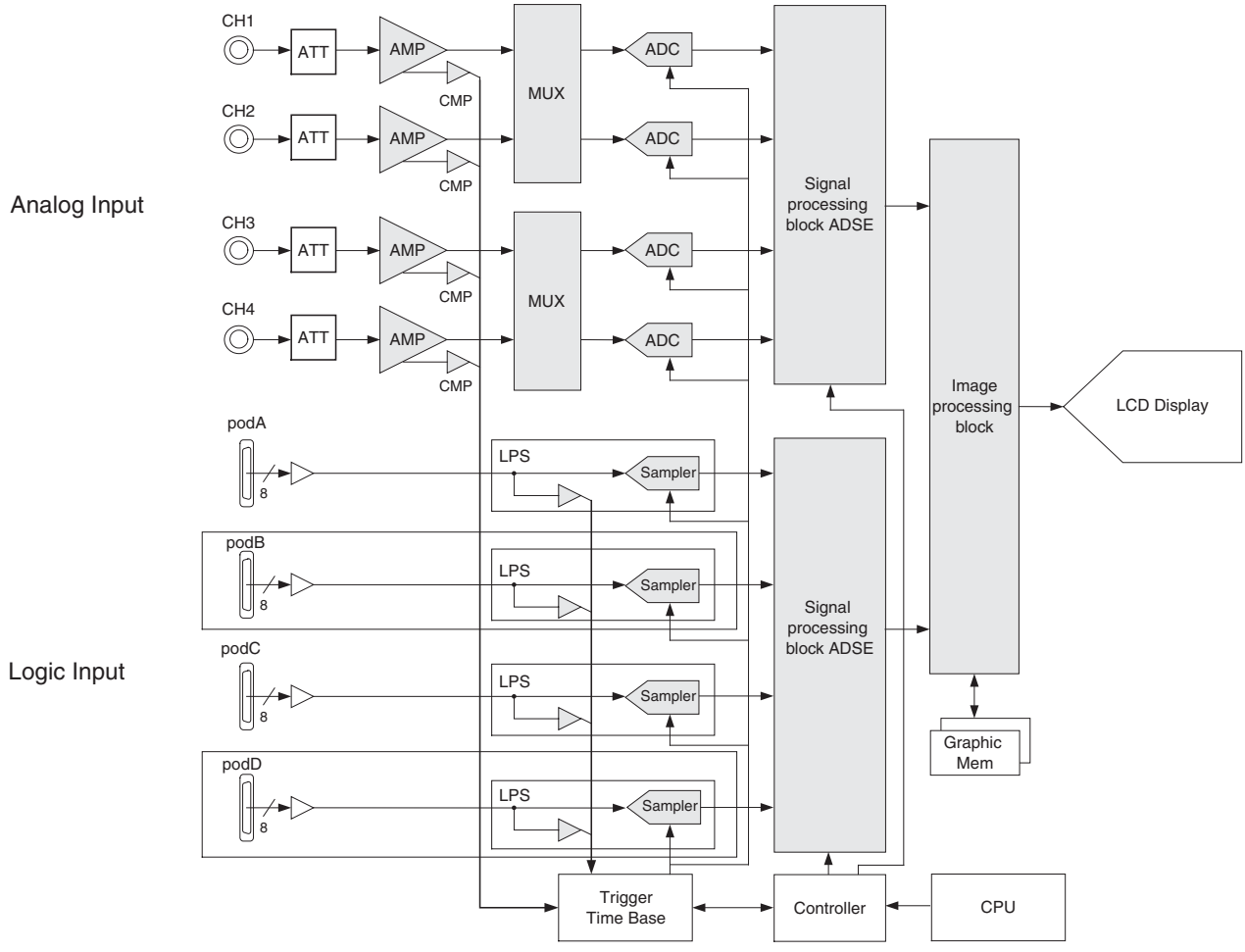

Figure 2 DL9700/DL9500 Series Configuration (DL9500 is pod A and C only)

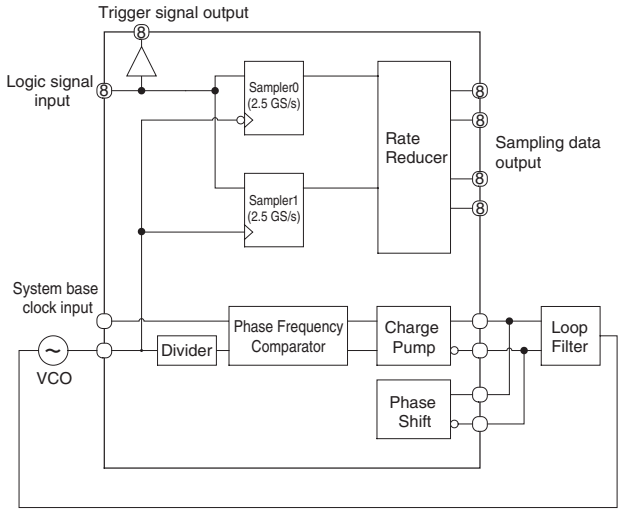

Figure 3 LPS (Logic Probe Sampler) Block Diagram

LPS (two in DL9500).

To more accurately track the timing of the maximum toggle frequency 250 MHz signal of the logic input, the DL9700/DL9500 series logic block has also been given the maximum sampling rate of 5 GS/s. The rising edge and falling edge times of the 250 MHz signal are generally low at 0.6 ns or less. To track this edge accurately, sampling data of one or more point is required within the rising and falling times. The 5 GS/s maximum sampling rate of the DL9700/DL9500 series is able to obtain sampling data of two or more points, allowing even more accurate timing analysis and waveform display.

FEATURES

The following describes features of the DL9700/DL9500 series.

(1) Trigger function

In addition to the rich variety of analog trigger functions, trigger conditions can also be set with logic signals as the source. This allows all four channels of the analog input to be used for signal integrity evaluation and analysis by assigning logic signal inputs to trigger sources in the analysis of analog/logic mixed circuits. Furthermore, setting complex trigger conditions by combining analog and logic inputs is able to accurately track the target timing in mixed signal analysis.

Table 2 Main Specifications of LPS

Item	Specifications
Number of logic input signals	8 bit
Used process	Si Bipolar
Number of used gates	Approx. 1K
Package	27 mm□ EBGA, 356 pins
Power supply voltage	±2.5 V
Power consumption	Approx. 3.9 W, typical

Figure 4 Logic Signal Grouping Setting Screen

(2) Group and Mapping

Figure 4 shows the logic signal grouping setting screen. The DL9700/DL9500 series is capable of grouping 32/16-bit logic input signals into a maximum of five groups. The bus display, state display, and D/A conversion calculation analysis, etc. described later are executed in units of these groups.

There is no restriction on the number of bits of each group, and all 32-bits can also be assigned to one group. This setting can easily be set and changed using the graphical interface. This means that even if concerned signals change during the use of the bus display, this can be dealt with by changing only the group mapping; there is no need to change the connection of the logic input signal.

(3) Bus display

Figure 5 shows an example of the bus display of logic signals. 8-bit binary counter outputs ([A7: A0]) are displayed in hexadecimal in Group 4. ADSE processing displays the bus display without any loss in the high speed waveform update rate. The bus display provides good visibility of multi-bit logic input data, and combination of the state trigger and search described later realizes speedy analysis.

Figure 5 Bus Display of Grouped Logic Signal

Figure 6 State Display of Logic Signal

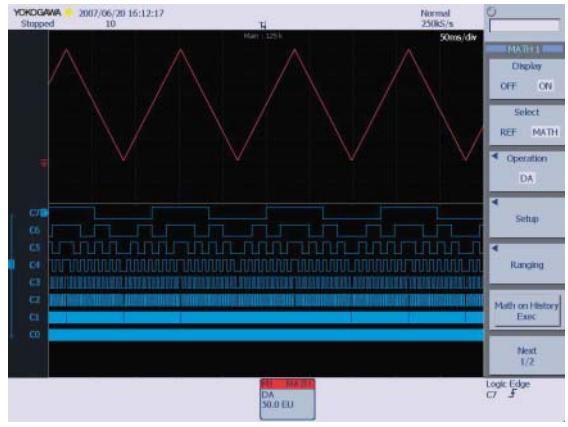

Figure 7 D/A Conversion Display

(4) State display

Figure 6 shows an example of logic signal state screen. By determining the state of the data ([D7: D0]) at the rising edge of the signal (A0) selected for the clock, glitches causes by jitters and noise of input signals can be removed to display the correct state. This function allows analysis at the clock reference of the measured circuit on the DL9700/DL9500 series like the logic analyzer. As state display is also internally processed in the ADSE, it can be displayed maintaining the waveform update speed.

(5) D/A conversion

Figure 7 shows an example of D/A conversion of 8-bit signals. Logic signals can be D/A-converted by group, and displayed in the analog display area. This is useful as it enables easy comparison of the input/output waveforms of the D/A conversion circuit, A/D conversion circuit, and the peripheral circuits.

Furthermore, by combining the D/A conversion output together with waveform analysis functions such as histogram function, sophisticated analysis of the linearity characteristics, etc. of the D/A conversion circuit and A/D conversion circuit is possible on just the DL9700/DL9500 series alone.

CONCLUSION

Yokogawa has released a new highly functional compact DL9700/DL9500 series of mixed signal oscilloscopes with four analog input channels and 32/16-bit logic input.

Both the analog and logic inputs are able to take in sufficient data by high speed sampling of 5 GS/s maximum and 6.25 M word long memory. And by using high speed signal processing engines, high speed display and update of 25,000 waveforms/sec maximum has been realized. The DL9700/DL9500 also comes with sophisticated analysis functions required in development, such as triggers on combination of analog and logic inputs, automatic measurement of waveform parameters, and D/A conversion.

By adding optional probes, and serial bus analysis and power supply analysis functions, input signal analysis of various specifications and standards can be realized on just one oscilloscope.

We hope that the DL9700/DL9500 series of mixed signal oscilloscopes will be used to be the best debug tool for both hardware and software engineers in the development of embedded devices, whose market is expected to continue growing even more. ◆

REFERENCE

(1) SUGIHARA Yoshinobu, et al., “DL9000 Series of Digital Oscilloscopes,” Yokogawa Technical Report, No.40, 2005, pp.1-4