PHOTONIC MEASUREMENT AND CONTROL TECHNOLOGIES

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We have developed compound semiconductor devices and are supplying them to the optical communications systems market in the form of ultrahigh-speed modules. We have also built an optical packet network system using the newly added ultrafast switching devices.

The ultrahigh-speed optical communications modules comprising HBT (heterojunction bipolar transistor)-based integrated circuits, including driver amplifier modules for optical modulators, logic and photodiode modules, have achieved transmission rates higher than 40 Gbps. The yield and reliability of the integrated circuits are sufficiently high for Yokogawa to market these modules as key components for telecommunications infrastructure.

Optical packet network systems, which directly switch optical signals on a packet basis without converting them into electrical signals, are considered the ultimate goal for high-speed, high-capacity optical networks but unrealistic until around 2015. However, we have succeeded in conducting the world's first image transmission using the network system by focusing on its application to LANs in order to relax the technical requirements and by using the latest compound semiconductor technology.

I COMPOUND SEMICONDUCTOR TECHNOLOGY APPLICATION TO OPTICAL COMMUNICATIONS

INTRODUCTION

With the spread of the Internet and expansion of data communication, the need for transmission capacity for both long- and short-distance communications has been growing in recent years. In backbone network communications, technology for capacity expansion using Wavelength Division Multiplexing (WDM), and technology for high-speed transmission using Time Division Multiplexing (TDM), have been energetically developed and made suitable for practical application. In particular, from the viewpoint of high-speed communications, the development of 40 Gbps transmission technology for commercial use from the previous 10 Gbps transmission technology is a major advance and some applications are now at a stage for practical use.

In addition, the content of communication data has become diversified. For example, a diverse range of content needs has arisen, such as the instantaneous transmission of high-precision, high-definition video data, or the short-time transmission of a huge amount of data, or data transmission with low latency retaining a capacity for transmitting data.

Since 1983, Yokogawa has been developing ultrahigh-speed devices employing compound semiconductor substrates, i.e., gallium arsenide (GaAs) or indium phosphide (InP). This project has primarily aimed at producing higher performance and high-value-added test and measurement instruments to the market, by our fostering in-house development and improving the production capabilities of key components for these high-speed, high frequency measurement instruments.

In terms of the high-speed characteristics of compound semiconductor devices, the maximum oscillation frequency (f_{max})

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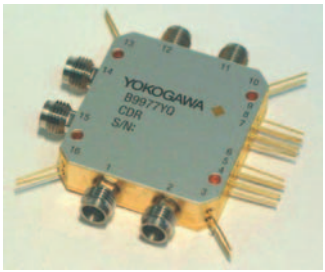

Figure 1 40 Gbps CDR Module
(37.3 × 34.4 × 10.4 mm)

Figure 2 CDR Subsystem
(200 × 100 × 24.2 mm)

of a transistor, an index for transistor performance, is 200 to 300 GHz. Moreover, compared to silicon semiconductors, compound semiconductor devices not only operate faster but also possess more flexibility in material selection and applicability to new devices[1]. In addition, the development of various types of optical semiconductor devices is relatively easy, owing to the physical properties of the materials. Accordingly, compound semiconductor technologies are suitable for the above purpose based on these facts. The devices that have been developed are utilized in various Yokogawa Group products and have been contributing to industrial society.

Furthermore, because compound semiconductor technologies are applicable not only for measurement-specific applications within the Yokogawa Group, but also for devices for the communications infrastructure, we have established in-house development and production lines for electronic devices[2] and optical devices for 10 Gbps and 40 Gbps optical communications. For the communication infrastructure, the devices require not only high-speed transmission performance but also high reliability, which is determined on the basis of the required reliability for communications systems. In this article, we first give an overview of compound semiconductor technology, and then describe the assembly technology for packaging semiconductor chip(s) into a package.

While modules for optical communications such as mentioned above are commercially available on the communication infrastructure market as separate components, we are aiming at using the optical packet network systems that have been developed in parallel to enhance and expand our business in optical communications beyond components for communication equipment and systems by further developing featured devices such as optical switches, optical logic circuits and so on. Centering on a high-speed optical switch device with a switching rate of 1.3 to 1.4 ns, advances made in equipment design technology, network technology and software technology have in combination made possible the switching of optical packets that pass through optical fibers without converting them into electrical signals. This paper outlines an overview of this optical packet network system.

COMPOUND SEMICONDUCTOR DEVICE TECHNOLOGY

This chapter describes the electronic and optical devices we have developed using our compound semiconductor technology.

When electronic and optical devices are used in test and measurement applications, stable operations in broadband regions ranging from DC to ultrahigh frequencies, are generally required. This means devices must operate at an ultrahigh-speed frequency with less time fluctuation and low noise, including in low frequency ranges.

Yokogawa has selected heterojunction bipolar transistors (HBT) as the basic amplifying element for electronic circuits. For field effect transistor (FET) devices represented by high electron mobility transistors (HEMT), defects in the crystal surface and in the traverse mode of the wafer affect the low-frequency noise characteristics of the device, as carriers move parallel to the wafer surface. In addition, the backgate effect with a significant slow-time constant adversely affects the low frequency characteristics.

In the case of HBT, carriers move vertically to the substrate surface; thus, the low-frequency noise characteristic is not affected by crystal surface defects. In addition, HBT is free of the backgate effect and possesses other characteristics in addition to high speed, such as operation with the correct amplitude at the first pulse, even after a long interval.

Moreover, various characteristic electronic devices can be developed using compound semiconductor technologies, such as a Schottky barrier diode with a high cut-off frequency, a variable capacitance diode capable of controlling reactance by the applied DC voltage (a kind of Schottky barrier diode) and a resonant tunneling diode with the characteristics of negative resistance and ultrahigh speed responsivity.

Furthermore, integrated circuits (IC) can be designed by combining the above mentioned devices with various passive elements which are thin-film resistors, metal insulator metal (MIM) capacitors, and wiring layers.

When operating at an ultrahigh-speed frequency, IC design technology is essential because it is necessary to eliminate parasitic elements such as capacitance and inductance and to control lower capacitance and inductance conditions, and to configure a precise transmission line. We have already manufactured a device comprising approximately 3,000 elements, with a practical yield for mass production, and we also believe it is capable of coping with such ultrahigh-speed applications.

In optical devices, we have developed photodiodes as key devices. These photodiodes have a PIN structure formed on the InP wafer, and are designed to enable high-frequency operation. The important advantage of this configuration applies to operation over a wide wavelength band which enables the photodiode's high-sensitivity (from the O- to U-bands) to cope with all WDM bands,

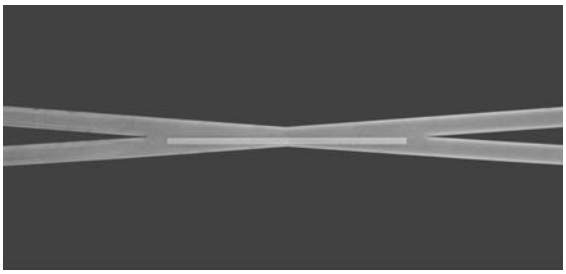

Figure 3 Waveguide Intersection in 2 × 2 Optical Switch Device (SEM Photo)

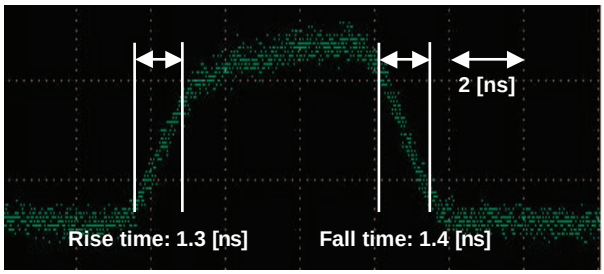

Figure 4 Switching Time in Optical Switch Device

and a service channel for line monitoring and maintenance.

However, even if these devices have good short-term characteristics, it does not mean that they are practical. In other words, long-term stable operation is necessary. From the outset, we have been very conscious of this need for long-term stability, and have conducted various reliability tests, paying much attention to the design of device structures. For example, we have conducted a high temperature bias test (an acceleration test in which heating takes place during operation) on a small integrated circuit which included HBT on the InP wafer, and the test time exceeded 30,000 hours in actual time. This period is equivalent to more than 250 years under normal operating conditions.

OPTICAL COMMUNICATION MODULE TECHNOLOGY

The compound semiconductor ICs described in the preceding chapter are semiconductor chips of several square millimeters in size. For the practical application of the chips, the technologies for implementing the chip(s) into a package, and for connecting internal electronic and optical signal lines with external connectors are very important because such packaging and assembly enormously influence the performance of a packaged component, called a “module”. A package consists of a metal or ceramic case, RF connectors, alumina substrates for internal transmission lines, low-frequency passive components and so on. Since operation at ultrawide frequencies ranging from the order of 10 kHz to 10 GHz is required for 40 Gbps application, frequency response must be flat not only in the RF band, but also over the whole band. It is essential, therefore, to properly select and connect passive components such as decoupling capacitors, bypass capacitors and RF blocking inductors. In the case of a photodiode, optical input signals via an optical fiber should be efficiently coupled to the chip.

To ensure the expected performance for long-term stable operations over a wide range of temperatures, it is necessary to consider thermal design with the intent of decreasing chip temperature. Yokogawa has employed a chip carrier made of copper tungsten, and developed an optimum design for parts layout. To use transmission lines on the alumina substrate at a high frequency, the lines must be designed paying particular attention to pattern width and to the bend pattern, while at the same time making compensation for parasitic elements. We have established our own standard design rules based on both computer simulations and actual measurements through verification using test patterns.

For assembly, as ensuring stable module performance in manufacturing is extremely important, we have managed and controlled the length of wire bonding and the amount of adhesive material such as Ag paste. In addition, we have established an optical design rule and an assembly process that satisfy both performance and mass productivity requirements. We believe our mission is development and releasing new technologies into the market as soon as possible. Therefore, we consider it indispensable to establish a stable manufacturing process—from pre-processing to post-processing, and to maintain the reliability and quality of the resulting products. We have been advancing steadily along this path.

Figure 1 shows a photograph of a 40 Gbps clock and data recovery (CDR) module as an example of an optical communication module.

We have also developed a subsystem comprising RF modules and LF peripheral circuits. Figure 2 shows a CDR subsystem that functions both as a clock divider and an amplifier, in addition to the functions of the above CDR module. From now on, we plan to shift our development objectives from single modules toward high-performance, high-value-added subsystems and systems.

OPTICAL PACKET NETWORK SYSTEM TECHNOLOGIES

In addition to the modules for optical communication described in the previous chapter, we have developed an ultrafast optical switch based on our compound semiconductor technologies. Figure 3 is an SEM photograph of the center portion of the switch. Two optical waveguides on a semiconductor substrate cross at a certain angle, and an electrode is installed in a portion of the intersecting area. Capitalizing on the effect that carrier density change due to current injection causes refractive index change, and whether the incident light beam travels straight or whether it is completely reflected can be controlled by the injection current.

Figure 5 Optical Switch Device Housing
(70 × 18 × 10.5 mm)

Figure 6 Optical Packet Switch
(362 × 75 × 404 mm)

Figure 7 Optical Media Manager
(426 × 88 × 576 mm)

In other words, the switching of optical paths can be controlled by electric signals at ultrafast speed because of the high mobility of the carriers in the compound semiconductor. Figure 4 shows the result of an experiment with a switching time of 1.3 ns (rise) and1.4 ns (fall).

This means that the optical path switching speed of less than two nanoseconds (two-billionths of a second) is a million times faster than that of other optical devices based on such principles as movable MEMS mirrors or the thermooptic effect for the refractive index change.

Taking advantage of this, optical packet-by-packet switching is the core technology of optical communication systems. Figure 5 shows an implementation of an optical switch device. The module has two input fibers, two output fibers and an electronic input connector. Furthermore, to integrate more functions into one chip, we have been able to successfully develop and install 4 × 4 and 6 × 6 switches, as well as the 2 × 2 switches shown in Figure 3, into the optical packet switch.

In addition we have developed an optical buffer memory to prevent packet collisions by combining delay optical fibers with an optical switch. Furthermore, using compound semiconductors, we have successfully developed core components essential for an optical packet network system, such as a device for recognizing the optical label of an optical packet and a device for burst-mode clock recovery, and then we have developed optical packet switches shown in Figure 6.

In optical packet networks, we use our own protocol to effectively operate the whole system using optical switch devices. For this reason, we have also developed an equipment called an optical media manager that functions as a gateway between a conventional network and our own optical packet network (see Figure 7). In the current configuration, the optical media manager uses one 10 GbE interface and 4 GbE interfaces as conventional interfaces. In addition to these Ethernet interfaces, we are also working on the development of a high definition serial digital interface (HD-SDI).

When switching optical signals with conventional technology, the signals are first converted to electrical signals, then packet switching is performed by the electronic switching circuit, and then the electrical signals are re-converted to optical signals for output. On the other hand, using our optical packet-switched network, optical packets are switched in an optical domain. Consequently not only is switching latency very short, but power consumption is also reduced.

Generally, it is predicted that these optical packet networks will not be practically realized until 2015, but we believe that practical optical packet network systems can be built earlier than expected by focusing on the high-end Local Area Network (LANs) field, and not concentrating on general-purpose systems in the initial stages. Currently, we are revising and adjusting the optical packet network system we have developed based on feedback from customers and focusing on our earlier practical applications.

CONCLUSION

In the preceding chapters, we have outlined the status of the developments we have made in our optical communication R&D activities. To continue providing the devices, subsystems and systems mentioned above, it is essential to establish a reliable manufacturing system and a stringent quality control policy. From the early stages of development, we have established functions and systems concurrent with R&D activities to dependably produce quality products agilely. In addition, we constantly strive to take full advantage of feedback from customers for our R&D activities through our sales and marketing operations. We take pride in our business approach with its emphasis on a high-speed development cycle of our R&D activities, as well as high-speed devices. We are confident that we will be able to make significant contributions to one of the most important social infrastructures by providing useful devices, modules, subsystem equipment and network systems in the optical communication field.

To develop business based on the achievements of our R& D activities centering on compound semiconductors, we are constructing a new manufacturing facility[3] that will go into production at the end of 2006. As described in this paper, we aim to continue our concurrent development of technologies and various business activities in our quest to consistently supply innovative, high quality products. ◆

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II DEVELOPMENT OF ULTRAHIGH-SPEED OPTICAL COMMUNICATIONS MODULES

INTRODUCTION

Electronic devices fabricated on compound semiconductors using substrates such as gallium arsenide (GaAs) and indium phosphide (InP) are characterized by high speed and high breakdown voltage and are being studied in various research and development institutions. However, these institutions seldom have a full-scale organization taking the process from development of state-of-the-art technologies to practical use. Recently, research of silicon semiconductors employing silicon germanium as the base material of the transistor is increasing due to their high speed and high integration properties. Compound semiconductors are superior to them, however, in terms of breakdown voltage. In addition, they are superior in performance characteristics with an operational margin because the communication data formats usually have redundant bits for FEC (Forward Error Correction) that cause the bit rate to increase in actual operations. Furthermore, they are essential for optical communication because they make it possible to develop a variety of optical devices.

As our first target, we have developed a module for a baud rate of 40 Gbps and have applied this technology to a 10 Gbps module. From the viewpoint of compound semiconductor device technology, this paper describes the up-to-date development of electronic devices and photodiodes characterized by long wavelength and high frequency bands, focusing on the HBT (Heterojunction Bipolar Transistor). This paper also describes the structures and properties of the packaged driver module, the logic module and the photodiode module.

COMPOUND SEMICONDUCTOR DEVICE TECHNOLOGY

Our compound semiconductor process focuses on 4-inch wafers for both electronic and optical devices. The main electronic devices have an HBT mesa structure, with a vertical construction wherein their emitters are placed at the top. Moreover, the Schottky barrier diode, thin-film resistor, thin-film capacitor and 2-layer interconnections

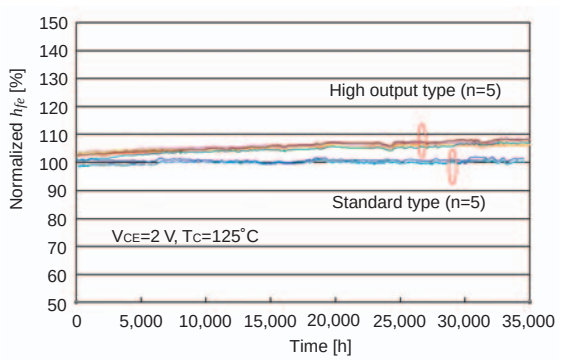

Figure 1 Trend in Continuous High-Temperature Bias Tests

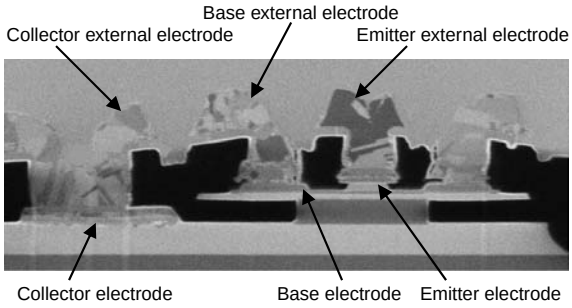

Figure 2 Device Cross Section (Side Base Voltage Supply)

(gold) can be produced as large scale integration (LSI) chips[1][2][3].

Since high reliability is required of devices in the optical communication field, we have confirmed the stability of HBT through the conduction of a high temperature bias test. (This is an acceleration test where the ambient temperature is increased up to 125˚C while power supply voltage is applied.) As shown in Figure 1, the normalized h_{fe} (assuming the initial value of the grounded emitter to be 100%) is significantly stable even after 30,000 hours. Hence HBT can be considered fully stable as this duration of time is the equivalent of 250 years at room temperature, which demonstrates sufficient reliability. In addition, we have conducted an acceleration test on a photodiode chip at a high temperature of 175˚C, and have confirmed that the dark current is small enough for stability of the photodiode chip.

In recent device development, we have employed a new method for placing external electrodes along a base structure (Figure 2) rather than in conventional positions and instead of according to the InP-HBT base electrode lead method. We have confirmed that f_{max} (maximum oscillation frequency) increases by 50 to 100 GHz, resulting in significant performance improvement as seen in the f_{max} changes in Jc (collector current density) as shown in Figure 3. In InP-HBT which has a double hetero junction structure, we have optimized the doping concentration and collector thickness, so that the breakdown voltage improves by 3 V compared with the conventional configuration as shown in Figure 4.

When a Schottky barrier diode is integrated with HBT, the collector layer is usually used for a Schottky junction. This structure can provide the full characteristics of a high-speed diode. In

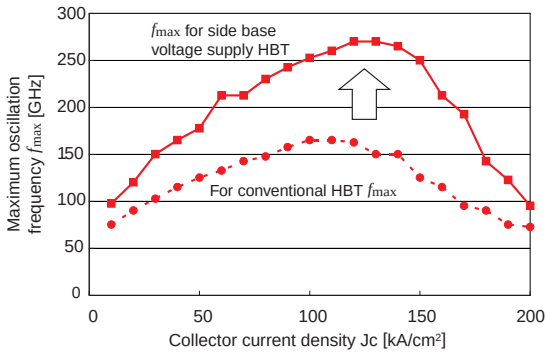

Figure 3 Collector Current vs. Maximum Oscillation Frequency Characteristics

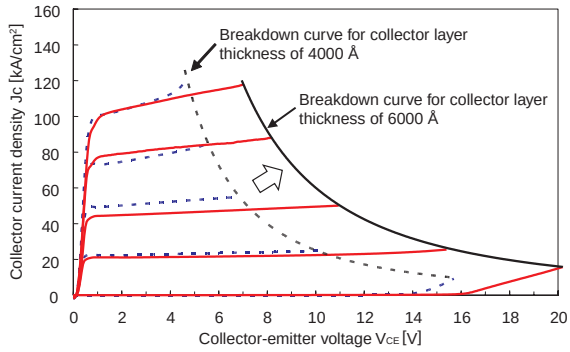

Figure 4 High Breakdown Voltage HBT

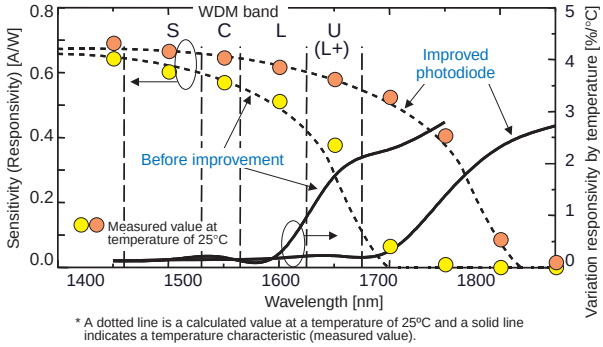

Figure 6 Photodiode Wide Wavelength Characteristics

addition, a variable capacitance diode with excellent characteristics can be created by optimizing the doping profile of the Schottky barrier diode. We have combined this variable capacitance diode and a transmission line to create a phase shifter that can control the phase relationship between the input and output sine waves through the applied DC voltage. Though data lines require an ultra-broad bandwidth like the driver and logic circuits shown below, the clock lines only require a single frequency, which means a circuit taking advantage of resonance can be employed. Figure 5 shows the characteristics on a wafer measured with the 20 GHz phase shifter.

In terms of photodiodes, we have developed and supplied devices for internal use such as WDM (Wavelength Division Multiplexing) monitors and spectroscopic analysis instruments. Taking full advantage of this technology, we have developed a new photodiode that meets the requirements for both high responsivity and wide wavelength. In this new photodiode, the vertical structure of the devices and the electrode structure dimensions have been optimized due to surface injection p-i-n InGaAs PDs. This enables them to meet requirements such as a wide wavelength, high frequency response and sensitivity. The characteristics shown in Figure 6 show the wavelength on the horizontal axis, and responsivity on the vertical axis, and indicate that the long wavelength characteristics of the new photodiode are superior to those of conventional photodiodes. Because they cover up to a WDM wavelength area called the U-band, they can transmit communication data or can assign so-called service channels (i.e., for control or maintenance data). As described below, this device has a frequency characteristic with a sensitivity of 50 GHz or more as a photodiode module and fully meets market needs.

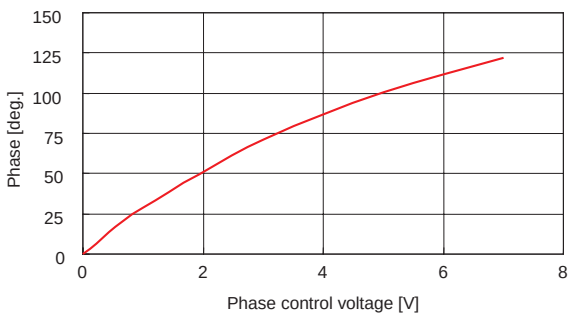

Figure 5 Phase Shifter Chip Characteristics
(Operating Frequency: 21.5 GHz)

DRIVER MODULE FOR 40 GHz OPTICAL COMMUNICATION

An optical modulator is employed to turn a series of optical signals of a single wavelength on or off when high-speed electric signals are used as input signals. The typical modulators for this purpose are EA (Electricabsorption) and LN (Lithum Niobate) modulators. The EA modulator is mainly employed for short-distance communication. We have developed a driver for this modulator as shown in Figure 7. This driver employs a differential signal for input and a single end signal for output. This enables the output terminal to directly interface with the EA optical modulator without external bias-T. We have employed a small GPPO connector as a connector for these high-speed electric signals because of its easy connection feature. This module is a multi-chip module comprising an input signal buffer and two distribution-type amplifiers. Figure 8 shows an NRZ (Non Return Zero) optical waveform of PRBS (Pseudo Random Binary Sequence) that can be obtained by combining the EA modulator with the EA driver. This is a so-called eye pattern, obtained by overwriting the response waveforms on various bit patterns. As the white area becomes larger in a waveform, it indicates the improved characteristic. In Figure 8, the PRBS length is 2^{31}-1 bits, and the bit rate is 39.8 Gbps. This driver is mainly used for VSR (Very Short Reach), i.e., it is used for transmission within a range of approximately 2 km.

Next, we'll discuss the LN modulator driver. The LN modulator is mainly used for backbone networks or metropolitan networks connecting big cities. The driver is also intended for the same application.

Various improvements have been made on the LN modulator in

Figure 7 Driver Module B9977XP for EA Optical Mmodulator
(16 × 29 × 7 mm: excluding protrusions)

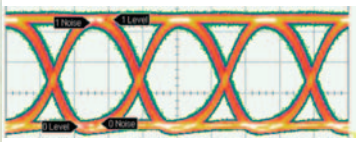

Figure 8 EA Modulator Optical Output Waveforms
(40 Gbps)

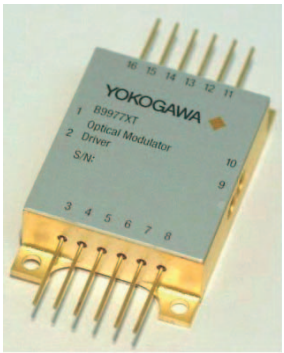

Figure 9 Driver Module B9977XT for Low V LN Optical Modulator
(23 × 27 × 8.4 mm: excluding protrusions)

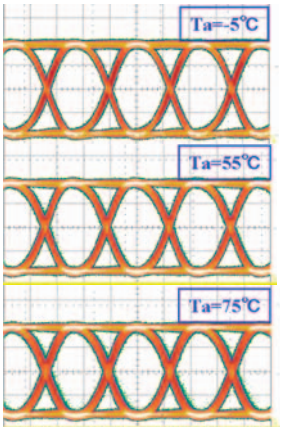

Figure 10 Low V LN Optical Modulator Output Waveform (43 Gbps)
LN modulator: Fujitsu FMT7935EZ(H74M-5208-J107)

various places, and now a low V LN modulator which features low driving voltage at the 40 Gbps band is available. Figure 9 shows a driver for this LN modulator. This driver has a DFF (D-Type Flip Flop) for retiming in an input portion and employs a differential driving method for output suitable for the LN modulator. In this case, we have also employed GPPO connectors for miniaturization. Figure 10 shows a 43 Gbps optical waveform (PRBS length: 2^{31}-1 bits) obtained by employing the low V LN modulator. This figure shows the good characteristics that can be obtained by changing the ambient temperature, and we have confirmed that good waveforms can be obtained over a wide range of temperatures. In addition, we are developing optimal driver modules and clock-related circuits to cope with various modulation formats other than NRZ which are undergoing research and development in various places.

LOGIC MODULE FOR 40 Gbps OPTICAL COMMUNICATION

The multiplexer, demultiplexer and flip-flop for conversion between 40 Gbps and other Gbps are called the logic modules. Both the multiplexer and the demultiplexer have about 2,000 devices integrated and they boast good yield and high-speed characteristics[1][2][3].

In addition, DFF has been packaged in the case shown in Figure 11

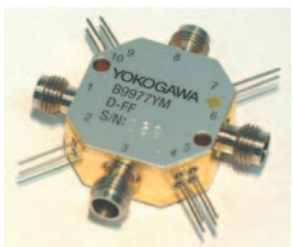

Figure 11 DFF Module B9977YM
(25 × 25 × 9 mm: excluding protrusions)

Figure 12 DFF Module Output Waveforms
(43 Gbps)

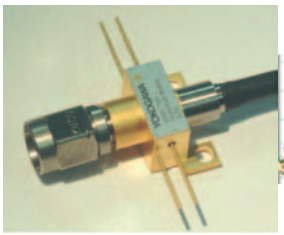

Figure 13 Photodiode Module B9977XR
(5.5 × 12.7 × 8.7 mm: excluding protrusions)

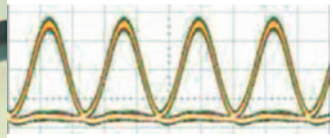

Figure 14 Photodiode B9977XR Output Waveforms
(43 Gbps RZ signal)

and the eye pattern shown in Figure 12 has been obtained. This eye pattern is an output waveform of the DFF module when a data signal of PRBS length 2^{31}-1 is applied to the DFF module at a rate of 43 Gbps. It shows good characteristics in that the RMS jitter is 600 fs (femtoseconds) and Eye S/N is 23.8. A T-type flip-flop (TFF), which serves as a frequency divider for half frequency, is assembled in the same package, and its maximum toggle frequency is 56 GHz in a dynamic TFF and 34 GHz in a static TFF. This is beneficial to the construction of systems using various clocks.

For clock data recovery, we have developed a unit comprising a PLL clock recovery function that contains a phase detector for flip-flop circuits, a voltage control oscillator (VCO), a feedback circuit and a data recovery function which is implemented by a retiming DFF. This unit has facilitated the confirmation of good operation characteristics, with the RMS jitter of a recovered clock being 290 fs for data input at a rate of 43 Gbps.

40 Gbps PHOTODIODE MODULE

The configuration of a lineup of photodiode modules that have the above photodiode mounted in the package comprises a single photodiode, a diode with an amplifier (electronic circuit), etc. Figure 13 is an external view of such a package containing a single photodiode. As this kind of photodiode module is mainly used for development, we have employed a V-type connector because of its good repeatability, taking into consideration that the output connector will be connected and disconnected repeatedly.

Figure 14 shows a waveform measured when a 43 Gbps RZ (Return Zero) signal is received by this photodiode module. It shows good characteristics in that the RMS jitter is 240 fs and Eye S/N is 26.9.

As described earlier, the characteristic of wavelength versus

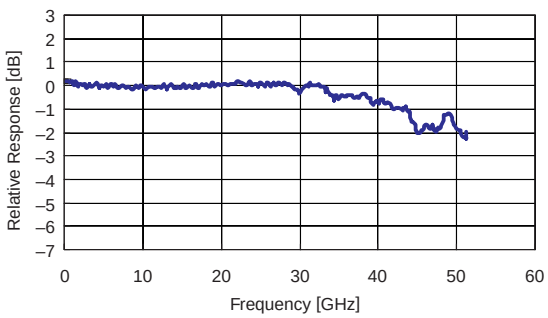

Figure 15 Photodiode Frequency Characteristics

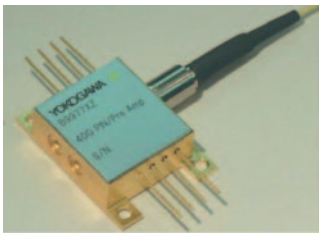

Figure 16 Photodiode Module B9977XZ with an Amplifier
(19.2 × 19.1 × 8 mm: excluding protrusions)

sensitivity is extremely good. In terms of speed, we have confirmed that a good RZ waveform can be obtained as shown in Figure 14, and there is a bandwidth of 50 GHz or more as shown in Figure 15. The measured result obtained by the heterodyne method using optical beats indicates the presence of a sufficient bandwidth.

Figure 16 shows a photodiode module integrated with a photodiode, a TIA (Trans-Impedance Amplifier) and an LA (Limiting Amplifier). We have employed GPPO connectors as output connectors from the viewpoint of VSR (Very Short Reach) application and mass production. In addition, we have developed a module where the photodiode device and TIA without the LA are mounted in the same package.

10 Gbps OPTICAL COMMUNICATION MODULE

Figures 17 and 18 show photos of external views of 10 Gbps modules developed using compound semiconductor technology. Though these modules were developed based on 40 Gbps technology and have been slightly modified, we have confirmed that their waveform quality and characteristics are good.

Figure 17 shows that both output amplitude control (1-12 Vpp) and phase control (360 degrees or more) can be performed using the 10 GHz clock driver employed in the 10 Gbps transmission system.

Figure 18 shows a surface mount package employed in the 10 Gbps photodiode. A high-speed electric signal output is passed through a CPW (Co-planar Waveguide) transmission line which can be directly connected to a printed circuit board. Figure 19 shows the output of a 10.7 Gbps RZ output waveform where the wavelengths and temperatures have been changed. The technology discussed earlier has already been applied to in-house products and its typical in-house application is as a 10 Gbps driver designed for measuring instruments. This driver has a

Figure 17 10 GHz Clock Driver B9977XX
(25.4 × 35.6 × 10.5 mm: excluding protrusions)

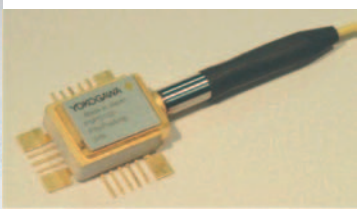

Figure 18 10 Gbps Photodiode B9977XY
(10.8 × 8 × 4 mm: excluding protrusions)

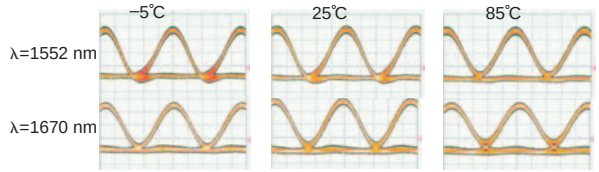

Figure 19 10 Gbps Photodiode Output Waveforms
(PRBS length 2^{31}-1, horizontal axis 20 ps/div)

retiming DFF output and a differential signal output. It can provide amplitude control, cross-point control and offset voltage control, and has already been mounted in our BERT (Bit Error Rate Tester) products such as AP9945 and AQ2200-601[4].

Focusing on an optical communication backbone system as our target system, we have developed a 10 Gbps high-end module by using 40 Gbps technology, thereby extending the application of compound semiconductor technology.

CONCLUSION

This paper has introduced optical communication modules using compound semiconductor devices as key components. These modules are still in the process of design optimization, taking advantage of the newly-emerging 40 Gbps communication market. Next, we intend not only to refine these modules to facilitate mass production, but also to research and develop the next-generation communication modules.

In addition, we will continue to supply devices and modules for in-house groups of Yokogawa Electric Corporation so that they can continue to provide a variety of high performance, highly functional products, thereby contributing to the communication world.

Furthermore, we are confident that compound semiconductor technology applies to optical packet network systems and will keep playing a key role as a fundamental technology in that field.

We will make continued efforts in development and aim to provide valuable, high performance modules worldwide. ◆

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III DEVELOPMENT OF 40 G OPTICAL PACKET NETWORK SYSTEM 'ynet™'

INTRODUCTION

According to public data from an Internet Exchange (IX), the volume of communication data traffic through the Internet more than doubles yearly[(1)]. With an approach that processes this growing data traffic using conventional technologies, the progress of development in electric circuit technology will be overwhelmed by the increasing traffic volume, and the processing speed of electric circuits will form a communications bottleneck. In addition, it is said that proposed countermeasures to this bottleneck situation, such as the advanced development of faster processing electric devices and parallel processing technology, may result in an unacceptable increase in power consumption. To cope with these problems, there is high anticipation that photonic network technologies will present technical solutions as a key solution technology. Among many proposed schemes thus far, the ultimate goal is an optical packet network that switches each optical packet in an optical domain without converting the optical packet to electrical signals. Core technologies for optical packet networks are actively under development in universities and public research organizations in various countries, and deployment is slated for 2015 or later[(2)].

In general, the above scenario refers to the so called “core” or “backbone” communication network systems. The same can be said, however, of local area networks (LANs), since the volume of in-house data traffic for enterprise is also increasing rapidly, with a trend to the digitalization of diversified information. This issue is especially relevant to packet switching in IX (the peak traffic speed in one of the representative IXs, i.e., JPIX, exceeded 65 Gbps in about July 2006[(1)]), the digitalization of image sources and the in-house digital distribution systems of broadcast TV stations that in Japan are being forced to change from an analog to a digital broadcasting system, and the in-house distribution system of digital cinema theaters.

Considering these situations, it seems evident that LAN systems will need optical packet network systems rather earlier than the core networks will. For this reason, Yokogawa has targeted the LAN field, and has proposed the optical packet network ‘ynet™’. By limiting the application field to LAN networks, some technical requirements are eased in comparison with communication in the core system. This is due to 1) short distance communication being acceptable, 2) the scale of the assumed network being smaller, and 3) protocol standardization not being necessary. This article outlines the ynet™ system, the world's first optical packet network system that has actually proven workable in real communication traffic and the core technology[(3)] comprising the ynet™.

OPTICAL PACKET NETWORK SYSTEM 'ynet™'

Outline of the Network System

The successfully proven optical packet network ynet™ has a ring network topology (Figure 1) and consists of optical packet switches (Figure 6 in the article “I Compound Semiconductor Technology Application to Optical Communication”, p.38) and optical media managers (Figure 7 on the same page). Three optical packet switches are connected by a single optical fiber and comprise a ring network. Each optical packet switch is connected to an optical media manager with two optical fibers, one of which is for transmission and the other is for reception. The optical media manager functions as a gateway between conventional interfaces such as Ethernet and ynet™. The optical packet switch either directly adds optical packets from an optical media manager to the ring line (without converting them to electric signals), or drops optical packets from the ring line to the optical media manager. The ynet™ functions as an asynchronous system. Unlike conventional devices for optical communications that only require good RF characteristics, in an asynchronous system the devices require good DC and LF characteristics as well. We adopted the asynchronous system, however, because we were confident that our compound semiconductor technologies were capable of realizing such devices.

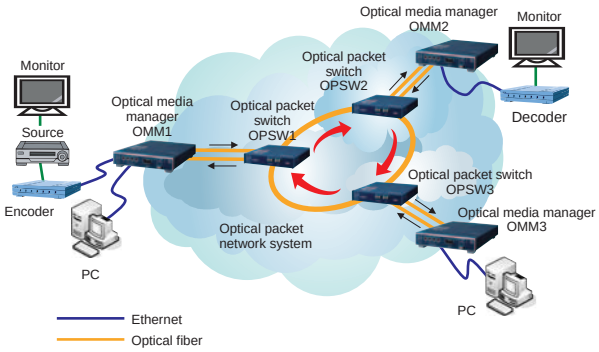


Figure 1 Optical Packet Network System 'ynet™'

Optical Media Manager

The developed optical media manager model has 4 Giga-bit Ethernet (GbE) ports and one 10 Giga-bit Ethernet (10 GbE) port. Figure 2 shows its internal configuration diagram. The Ethernet

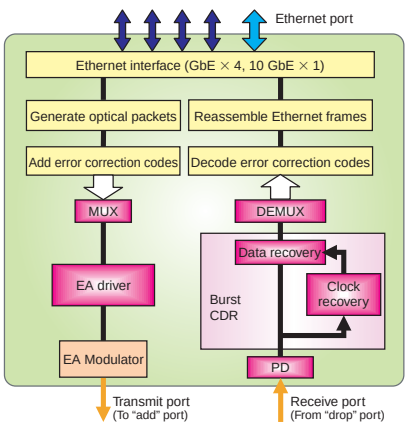


Figure 2 Block Diagram of Optical Media Manager

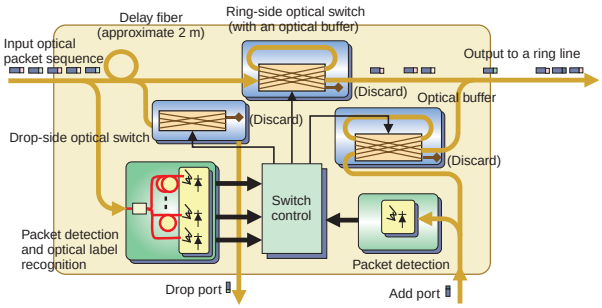


Figure 3 Block Diagram of Optical Packet Switch

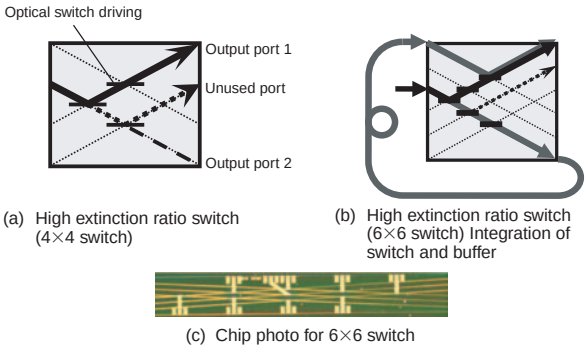


Figure 4 Highly Functional, High-Performance Optical Switch

interface functions as a layer 2 (L2) switch. The optical media manager automatically learns a look-up table between MAC addresses and ynet™ addresses and generates an optical label, so that users don't have to be aware of the optical packet network.

In this structure, the optical media manager generates optical packet data from a received Ethernet frame, encodes the data with a forward error correction (FEC) algorithm, then multiplexes the data to 40 Gbps and transmits the data as optical packets through an optical modulator. Received optical packets are converted to electric signals by a photodiode (PD) and the 40 Gbps data is recovered by a burst-mode clock and data recovery circuit (CDR). The recovered data are demultiplexed by a DEMUX and the data rate is down converted. After the FEC is decoded, the Ethernet frame is reassembled by the data and is output from a suitable Ethernet port. The structure of the optical packet will be introduced later section.

Optical Packet Switch

Figure 3 shows a block diagram of the optical packet switch. Each incoming optical packet from the ring line is divided into two individual packets by a splitter. One of these is input into an optical label recognition circuit, and the other is again split into two. After passing through a delay fiber that is about 2 m in length, one of these subsequently split packets is fed into a ring side optical switch and the other is fed into the drop-side optical switch. The length of the delay fiber is appropriate for the processing time required for label recognition and for switch control as explained below. The optical label recognition circuit reads the destination information carried by the optical packet's label, and outputs the result to the optical switch control circuit. The logic circuit from the optical label recognition circuit to the switch control circuit is a fixed logic circuit in order to minimize latency. The processing time of this circuit is currently about 10 ns.

If the optical label carries an optical address destined for other nodes, the ring-side optical switch is set for the output port and the drop-side switch is set for the discard port. Observing the optical packet switch externally, the optical packet seems to be passing through the switch. If the optical label carries an optical address heading to the node itself, the ring-side optical switch is set to the discard port and the drop-side switch to the drop port, so that the optical packet can be dropped. Our optical label structure can also be applied to broadcast and multicast. In these cases, both the ring-side and the drop-side optical switches are set to output ports. In addition, if an optical packet switch receives a packet carrying its own source, the packet is discarded as it has traveled the ring once.

A packet that is output from an optical media manager and is input to an add port of an optical packet switch is merged to the ring line through a coupler. At this time, if a pass-through packet is being output to the ring, packets collide with each other at the output port and are destroyed by the packet collision. To avoid this collision, a packet detection circuit and an optical buffer have been implemented to the add line as well as another optical buffer to the ring line. The optical buffer on the ring line is integrated with the ring-side optical switch. Each buffer is capable of buffering just one packet. The control logic to avoid collisions is based on a first-in first-out basis.

CORE TECHNOLOGIES

Optical Packet Switch Device

To develop a packet switching system, switching time must be sufficiently short compared to packet length. For up to 10 Gbps Ethernet technology, a frame gap must be 12 bytes. If 40 Gbps Ethernet were standardized with the same concept, the frame gap might be 2.4 ns (12 byte length of 40 Gbps). Therefore, we have set the goal of realizing a switching time for an optical switch device to 2.4 ns or less, assuming that 40 Gbps optical packets will be handled. The developed optical switch devices were described previously in the article, "I Compound Semiconductor Technology Application to Optical Communication". The switching time of the optical switch device is independent of the wavelength over a whole wavelength within C-band[4]. The extinction ratio of the optical switch is typically 15 dB, and its insertion loss is 10 dB. Most of the loss is the result of coupling loss between the optical fiber and the waveguide.

To improve the function and performance of the switch device, 4 × 4 and 6 × 6 switches integrating 4 or 6 waveguides, respectively, have been developed. By directing light beams leaked at a waveguide-crossing to an unused port using a 4 × 4 switch, the extinction ratio is improved to 25 dB or more. Furthermore, using a 6 × 6 switch, both extinction ratio

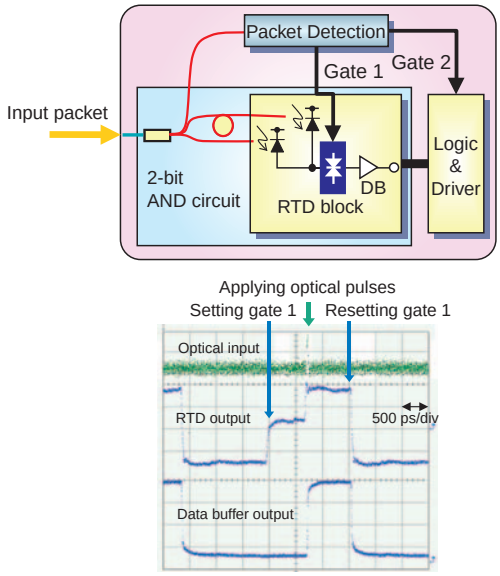


Figure 5 2-bit Optical AND Circuit Operating at 40 Gbps and its Operation Waveforms

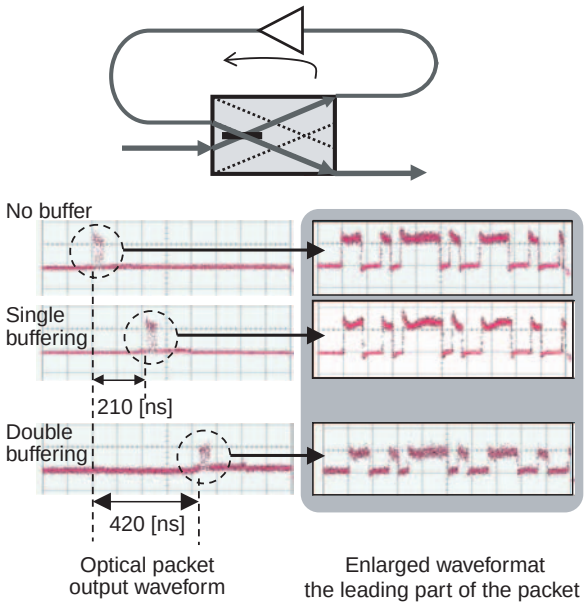


Figure 6 Basic Test Configuration for Optical Buffers and Experimental Results (Buffer Fiber Length: 42 m)

improvement and an optical buffer function can be realized in a single chip (Figure 4). The size of the 6 × 6 switch is about 12 × 1.2 mm.

Optical Label Recognition Circuit

Since a faster optical label recognition circuit directly results in shorter latency of the optical packet switch, its technology is very important. We developed an optical label recognition circuit based on a 2-bit optical AND circuit (Figure 5) combining an optical serial-parallel converter using delay fibers, fast photodiodes and a resonant tunneling diode (RTD). PDs connected in parallel are connected to an RTD block that consists of an RTD and an adequate electric load. If photocurrent exceeding a certain level is generated when the RTD block is biased (gate 1 is "ON"), the RTD block is switched from a stable state to another stable state. The switched new state continues until gate 1 goes OFF. Because Yokogawa's RTD[(5)] works at a switching rate as fast as 2 ps, it is easy for the originally developed RTD to latch pulses with a pulse of 25 ps width (1-bit width of 40 Gbps) if the PDs are sufficiently fast. The optical AND circuit is designed in such way that the RTD block switches by the accumulated photocurrent of two PDs when an optical pulse is input simultaneously into each PD.

Optical Buffer

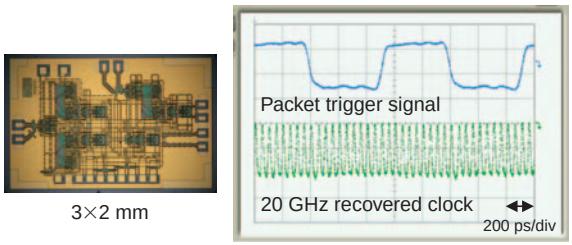
Although it is still a big dream for opticcal engineers to develop an optical memory technology in which optical signals can be stored as optical signals, it has not been realized yet. A practical alternative for an optical memory is to use an optical fiber as a delay line and input an optical signal into an optical fiber in order to delay the signal by the traveling time in the fiber. This alternative is called an optical buffer. Even in such a buffer, the speed of the optical switching device is a key factor because whether each packet is to be buffered or not should be controlled by the optical switch. Figure 6 shows a configuration of a basic experiment with an optical buffer, and its results. To compensate for coupling loss generated between the delay fiber and the optical switch device, an optical amplifier was used. As the waveforms show in Figure 6, we have confirmed that an optical buffer can delay and output optical packets by controlling the optical switch according to the theory.

Burst-mode CDR

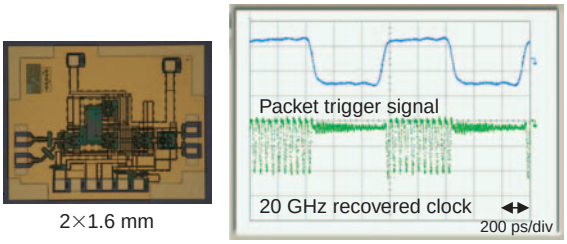
The most important device in the optical media manager is a burst-mode CDR. Recovering clock and data information from an optical packet itself that is input asynchronously, is required. We have newly developed two types of burst-mode clock recover (CR) ICs oscillating at 20 GHz using InP HBT technology. One is a constant oscillating type of burst-mode CR-IC wherein its frequency is locked to the reference frequency during no packet input. Its oscillation phase is rapidly adjusted to the edge of an optical packet detection signal. The other is a one shot oscillation type wherein oscillation begins at the same phase each time, triggered by an optical packet detection signal. Figure 7 shows photographs of these IC chips and the waveforms of oscillation at 20 GHz. The current system uses the one shot oscillation type CR with shortened absent durations of oscillation. Data can be successfully recovered without any preamble.

Optical Packet Structure

Figure 8 shows an optical packet structure designed to use device characteristics efficiently. An optical label consists of an optical frame delimiter, a destination ynet™ address and a source ynet™ address. The optical frame delimiter is in very simple "FF00" data. The ynet™ address has 1 byte length and its first bit



(a) Constant oscillating type



(b) One-shot oscillating type

Figure 7 Burst CR-IC Chip Photos and 20 GHz Oscillation Waveforms

is assigned for multicasting or broadcasting. The part following the subframe gap carries data to be recovered electrically and consists of a header (a delimiter, a destination ynet™ address, a source ynet™ address and other management information) and a payload. The length of the payload is set to 128 bytes in the current system. An Ethernet frame, which is longer than 128 bytes, is fragmented and stored in the payload section. Though the subframe gap does not have much significant meaning in the current system, it is inserted in anticipation of the future swapping of optical labels utilizing this gap.

DEMONSTRATION

We actually built the ring network shown in Figure 1, to demonstrate the simultaneous transfer of 2 image streams, namely a high definition (HD) TV image compressed with MPEG2, and a DVD image. The HD image stream is transferred from an MPEG encoder that is connected to OMM1, then to an MPEG decoder that is connected to OMM2; and the DVD image stream is transferred from a PC that is connected to OMM1 then to another PC that is connected to OMM3. The transferred image streams were monitored visually and the error rates were also recorded by the decoder and the PC. In this manner we could confirm that the data were correctly transferred.

The optical media manager is designed to fit into a rack that is 19 inches wide and 2U high (426 × 88 × 576 mm). The optical packet switch is smaller in size of dimensions (362 × 75 × 404 mm). Thanks to this compactness, a system consisting of 3 optical media managers and 3 optical packet switches is small enough it can be set on a display table at exhibitions. These compact sizes are a direct result of our compound semiconductor technologies.

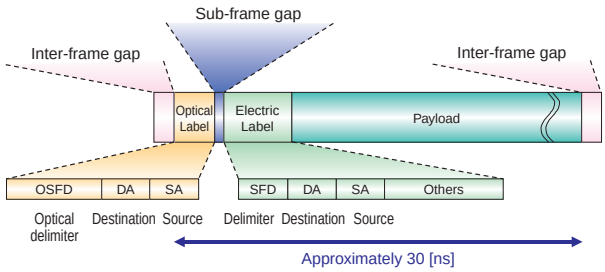


Figure 8 Optical Packet Structure

CONCLUSION

We have demonstrated image stream transfer using the ynet™ optical packet network that we have developed, and shown that an optical packet network can work well. On the other hand, it is true that there remain many issues which still present difficulties and which must be improved in the future, as we have developed the system focusing on actual speed in the system operation. More specifically, these issues include the evaluation of collision management function, the optimization of optical packet structure, the stabilization of the burst-mode CDR, developing programmable optical label recognition and the diversification of user interfaces.

Although there are many issues to be improved to realize practical implementation, we believe it is very significant that we have realized an operating optical packet network using real traffic. In future, we intend to address the above issues and aim to release commercial systems for practical deployment. ◆

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