FIELDBUS COMMUNICATION INTERFACE IC

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This paper introduces the recently developed fieldbus MAU (medium attachment unit) IC, which includes a power supply block, a transmitter block and a receiver block. The power supply block generates two regulated voltages from the powered bus. The transmitter block controls the rise and fall time of the bus signal so as to meet the fieldbus output timing requirements and outputs that signal to the bus. The receiver block includes a filter and comparators. In addition, the IC includes a low-power signaling function and a jabber inhibit function. A supply current of as small as 0.7 mA is achieved so that the IC can be used with field devices. The IC uses Yokogawa's 3-μm bipolar process and is housed in a 44-pin plastic quad flat package (QFP). This paper outlines the circuit configuration of the IC and the results of its evaluation.

INTRODUCTION

To configure a compact, low-power medium attachment unit for field buses, i.e., a fieldbus MAU, an IC comprising a power generator, transmitter/receiver and other functions is needed. While we at Yokogawa had already developed a fieldbus MAU IC[(1)], we have now developed another MAU IC that includes large-scale design changes made mainly to comply with the low-power signaling requirements of the fieldbus specifications. The following four major changes were made to the previous MAU ICs:

- Addition of low-power signaling function (reduction in the bus current during no transmission)
- Addition of jabber inhibit function (prohibition of transmission beyond a specific time period)
- Reduction in the number of external components
- Reduction in current consumption

The IC uses a 3-μm bipolar process with high-resistance polysilicon.

This paper explains the configuration of the new fieldbus MAU IC and also gives an evaluation of them.

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CONFIGURATION OF THE IC

Figure 1 is a block diagram of the fieldbus MAU IC and an example of its external connection. The fieldbus has both a low-speed (31.25 K bits/s) mode and a high-speed (1 or 2 M bits/s) mode. The IC discussed here supports the low-speed mode used by most field devices and basically consists of a power supply, transmitter, and receiver blocks, each of which are described below.

1. Power Supply Block

There are two standard methods for supplying power in a fieldbus system: a two-wire system (bus-powered) in which a signal line is also used to supply power and a four-wire system (non-bus-powered) in which the signal line and power line are separate.

In the two-wire system, a shunt regulator is necessary to derive power from the signal line. This power is used to operate the IC itself, as well as the sensor, CPU, communication control IC, and other components. On the other hand, digital circuits in field devices are often designed to operate at voltages lower than analog circuits. In order to meet this requirement, the IC also contains a series regulator. The voltage level of these regulators is either set internally or by using an external resistor. When set internally, the shunt regulator delivers a 5-V output, while the series regulator yields a 3-V output. These supply voltage levels are produced on the basis of the level of the voltage reference and

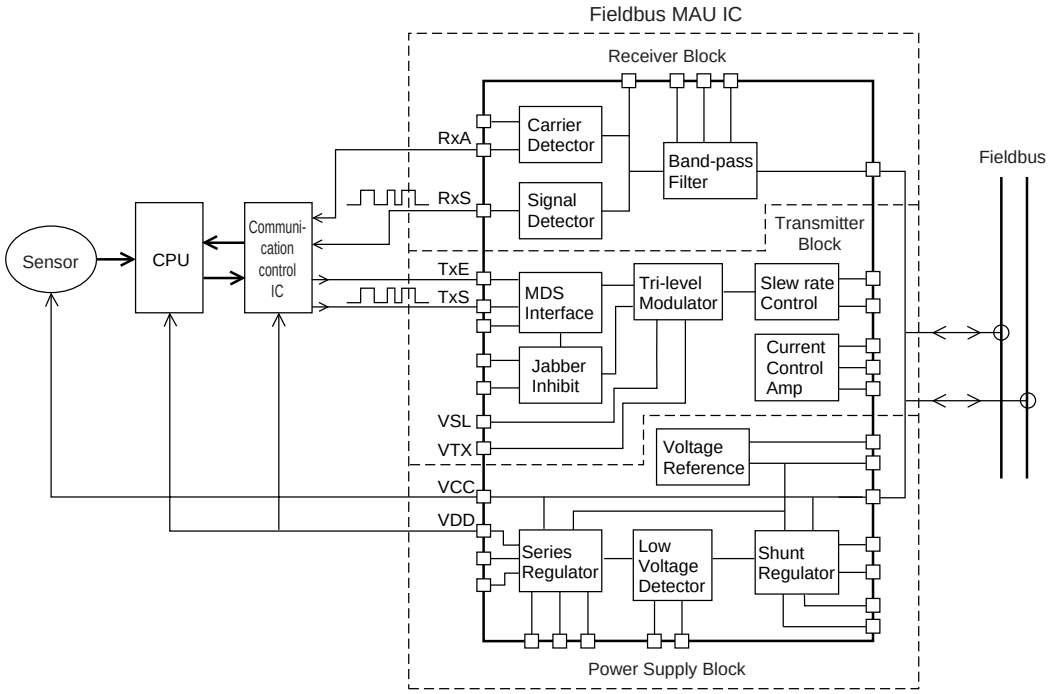

Figure 1 Block Diagram of Fieldbus MAU IC and an Example of External Connection

are well regulated against temperature variations.

The power supply block also contains two voltage detection circuits in order to monitor the output voltage of those two regulators.

2. Transmitter Block

The transmitter block consists of a medium dependent sublayer interface (an MDS interface), a jabber inhibit circuit, a tri-level modulator, a slew rate control circuit and a current control amplifier. The MDS interface receives digital transmission signals (TxE and TxS) from the communication control IC and generates a signal that controls the tri-level modulator.

The jabber inhibit circuit monitors the TxE signal using a timer. If the TxE signal remains active longer than the specified interval, the circuit judges the signal to be abnormal and stops transmission.

Figure 2 shows a circuit diagram of the tri-level modulator and slew rate control circuit. Using a current switch and an operational amplifier, this circuit feeds a three-state (static, low, high) analog voltage signal to the VDRV terminal.

If the IC is used in the basic configuration shown in Figure 1 and both VTX and VSL equal 0 V, then the level of the current sources, I (VSL) and I (VTX), will also equal zero. When the circuit outputs a static-state voltage level, SW1 and SW2 are

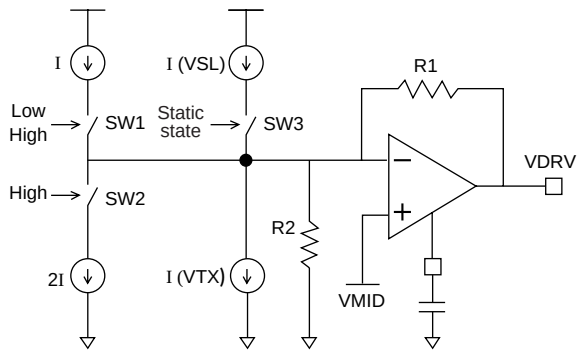

Figure 2 Circuit Diagram of Connected Tri-level Modulator and Slew Rate Control Circuit

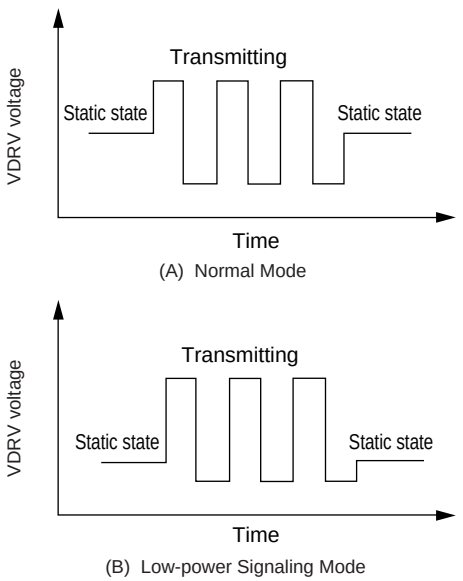

Figure 3 Waveforms at VDRV Terminal

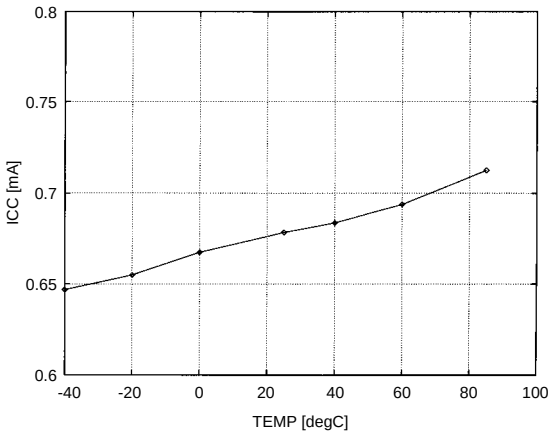

Figure 4 Current Consumption vs. Temperature

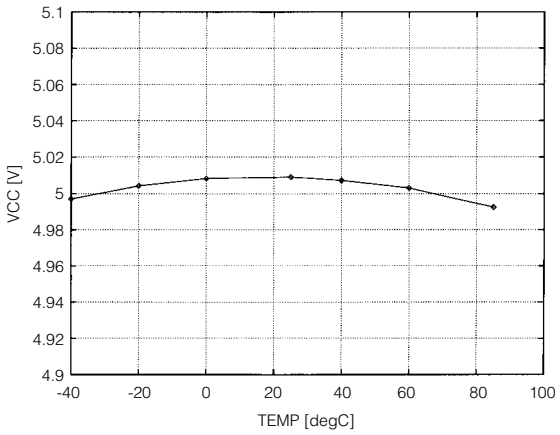

Figure 5 Shunt Regulator's Output Voltage vs. Temperature

turned off and the VDRV terminal's value is determined by the ratio of resistance R1 to resistance R2. When the circuit transmits a low voltage level, SW1 is turned on; when it transmits a high voltage level, both SW1 and SW2 are turned on. Thus, the three-state voltage levels, static, low and high, are output to the VDRV terminal, as shown in Figure 3 (A).

In order to change the static-state voltage level to achieve low-power signaling, a specific voltage level must be fed to the VSL terminal to set I (VSL). At the static-state voltage level, SW3 is on and only that level can be changed. As a result, we obtain the waveform shown in Figure 3 (B).

Conversely, if the quiescent transmitter consumes a relatively large amount of current, a specific voltage level is fed to the VTX terminal. The current I (VTX) thus produced continues to flow constantly, boosting the average current level.

The slew rate control circuit is designed to determine the rise time and fall time. The fieldbus standard specifies these parameters as less than 8 μs, and restricts the slew rate to less than 0.2 V/μs. This means the rise time should be greater than 4 μs for an output voltage of 1 V. In conclusion, both the rise time and fall time must be between 4 and 8 μs. The standard also requires that the rising and falling edges of a signal be symmetrical, since the bit cell jitter is specified as less than 0.8 μs.

In order to meet all of these requirements, the IC uses a method that determines the rise and fall time of a waveform from the operational amplifier's slew rate. A high-order filter is required when a filter is implemented in order to satisfy the rise and fall time and slew rate requirements discussed above. Our method is advantageous over the alternative one because it requires less external components; only one external capacitor needs to be added.

The current control amplifier is designed to receive the output of the slew rate control circuit to control the bus current.

3. Receiver Block

The receiver block consists of a buffer for bandpass filtering, a signal detector and a carrier detector.

The buffer for bandpass filtering is provided with two voltage followers so that a second-order bandpass filter can also be configured. The receiver block is also provided with resistors for filtering, which are not found on the earlier MAU IC. These reduce the number of external components. The frequency characteristics can be determined by means of an external capacitor.

The signal detector converts the filtered signal received to a digital value. The detector has a 15-mV hysteresis in order to suppress fluctuations in the output due to noise.

The carrier detector checks if there is any communication signal on the bus. If there is any signal higher than 100 mVp-p, the detector judges a carrier to be present on the bus and makes the RxA signal active.

4. Low-power Design

Since the IC is designed for use with field devices, its current consumption must be as low as possible. In order to meet this requirement, the current consumption of each circuit block is minimized and high-resistance polysilicon having a sheet resistance of 5 kΩ/□ is used for the computation resistors. Polysilicon is also used for the bias circuit, but in this case it is used in combination with a base diffusion resistor having a positive resistance-temperature coefficient. This approach minimizes temperature variations in the current consumption due to the negative resistance-temperature coefficient of high-resistance polysilicon.

5. Package

The new IC is available in a 44-pin plastic quad flat package (QFP) with a lead pitch of only 0.8 mm in order to meet the downsizing requirement.

RESULTS OF EVALUATION

Figure 4 shows the current consumption (ICC) versus temperature characteristics. As seen in the graph, the IC achieves a current consumption as low as 0.68 mA at 25°C. Furthermore, ICC is kept low over a temperature range as wide as -40°C to 85°C.

Figure 5 shows the shunt regulator's output voltage (VCC) versus temperature characteristics. As shown in the graph, the temperature coefficient is 30 ppm/°C and immune to changes in

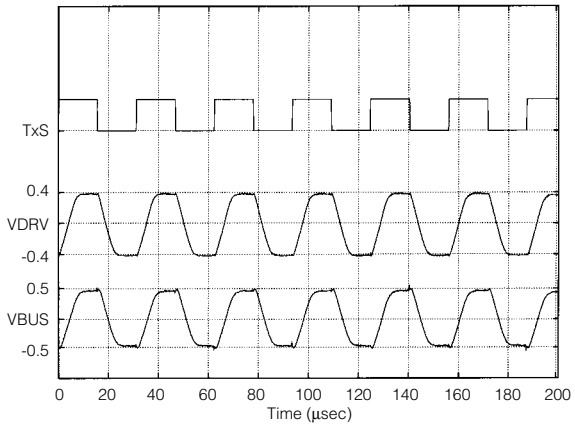

Figure 6 Signal Waveforms at Transmitter Block

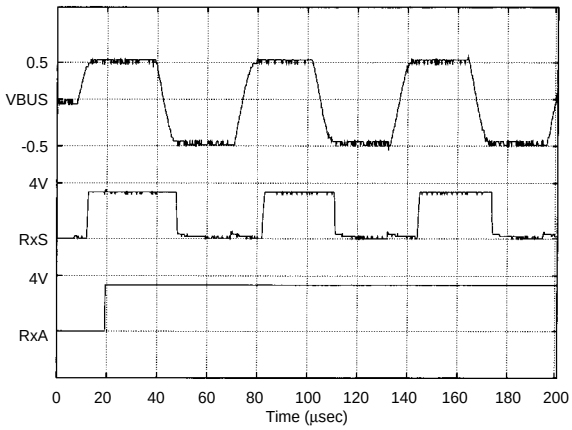

Figure 7 Signal Waveforms at Receiver Block

Table 1 Major Characteristic Parameters

Operating temperature range	-40°C to 85°C
Current consumption	0.65 mA
Shunt regulator:	
Output voltage	5 V ±5%
Output voltage temperature coefficient	30 ppm/°C
Sink current	25 mA (maximum)
Series regulator:	
Output voltage	3 V ±5%
Output voltage temperature coefficient	30 ppm/°C
Output current	20 mA (maximum)
Transmitter block:	
High level of output waveform	0.395 V*1
Low level of output waveform	-0.391 V*1
Waveform symmetry	4 mV
Receiver block:	
Carrier detection voltage	+51 mV, -52 mV*2

*1 Measured relative to the static-state voltage level (2.5 V DC).
*2 Measured relative to the AC ground level (2 V DC).

temperature.

Figure 6 shows the waveforms of signals observed when the transmitter block is in operation. In the figure, the signals are shown in the order of the TxS transmitted signal, the VDRV output signal of the slew rate control circuit, and the VBUS bus signal (from top to bottom). The TxS signal has a frequency of 31.25 kHz. The waveform of the VBUS bus signal has a rise and fall time of approximately 6 µs and a slew rate of 0.13 V/µs, carrying relatively small overshoots.

Figure 7 shows the waveforms of signals observed when the receiver block is in operation. In the figure, the signals are shown in the order of the VBUS bus signal, the RxS received signal, and the RxA carrier detector signal (from top to bottom). The waveform of the VBUS bus signal has a frequency of 15.625 kHz, indicating that the signal is one known as a preamble that occurs when signal receiving begins.

Table 1 summarizes the major characteristic parameters of the IC.

CONCLUDING REMARKS

As reported in this paper, we have developed a new MAU IC to support the low-power signaling requirements of fieldbus. This new fieldbus MAU IC uses our own 3-µm bipolar process and contains the features essential to fieldbus MAUs, enabling users to downsize the peripheral circuits of a fieldbus and reduce the amount of power consumption.

We expect that the new IC will become widely used in fieldbus-based devices developed in the future. ◆

REFERENCE

(1) Hasegawa Y., et al. "Fieldbus Transceiver IC." Yokogawa Technical Report, No. 2, pp. 63-66 (1995).