# General Specifications

Model NT351AJ
MELSEC Driver

**GS 34P02G01-01E**

## ■ GENERAL

*This MELSEC driver is an optional software package used to connect Mitsubishi Electric's MELSEC series of PLCs to the Versatile Data Server Software (VDS) system. It offers the following two connection methods.*

### ● EZSocket type

Connects to MELSEC by way of Mitsubishi's middleware EZSocket.

### ● Asynchronous type

Connects to the MELSEC sequencer CPU directly.

## ■ SYSTEM REQUIREMENTS

The system requirements follow those required for VDS specified in VDS Versatile Database Server Software, GS 34P02A02-01E.

*Note that the runtime version of MELSEC Driver does not allow the user to make or modify settings and only allows the monitoring.*

*Note that .NET Framework 3.5.1 must be enabled before installing Mitsubishi Electric middleware EZSocket. To enable .NET Framework 3.5.1 offline in a Windows 10 environment, the same version of Windows 10 installation media is required. Please contact the PC manufacturer about enabling the .NET Framework 3.5.1.*

## ■ EZSocket TYPE

The MELSEC driver incorporates EZSocket, Mitsubishi's communication middleware, for communication with Mitsubishi's MELSEC series.

### ● Interface Specifications

Applicable models: MELSEC A/QnA/Q/FX series
Connection interface: Serial, Ethernet, MELSEC NET II, MELSEC NET/10, MELSEC NET/H, CC-Link IE (formerly MELSECNET/G), CC-Link through EZSocket
Number of units connected: 32 max.
Function: Reading/writing of sequence devices

### ● Applicable Mitsubishi Models

**CPU Units**

A series: A0J2H, A1S, A1SH, A1SJ, A1SJH, A1N, A2C, A2CJ, A2N(S1), A2S, A2SH, A3N, A2A(S1), A3A, A1FX, A2U(S1), A3U, A4U, A2US(S1), A2USH-S1
QnA series: Q2A, Q2A-S1, Q3A, Q4A, Q4AR, Q2AS(H), Q2AS(H)S1
Q series: Q00J, Q00, Q01, Q02(H), Q02PH, Q03UDV, Q04UDV, Q04UDPV, Q06H, Q06PH, Q06UDV, Q06UDPV, Q12H, Q12PH, Q12PRH, Q13UDV, Q13UDPV, Q25H, Q25PH, Q25PRH, Q02(H)-A, Q06H-A, Q00UJ, Q00U, Q01U, Q02U, Q03UD, Q03UDE, Q04UDH, Q04UDEH, Q06UDH, Q06UDEH, Q10UDH, Q10UDEH, Q13UDH, Q13UDEH, Q20UDH, Q20UDEH, Q26UDH, Q26UDEH, Q26UDV, Q26UDPV Q50UDEH, Q100UDEH
FX series: FX0(S), FX0N, FX1, FX2(C), FX2N(C), FX1S, FX1N(C), FX3U(C)
L series: L02, L02S, L02S-P, L02-P, L06, L06-P, L26, L26-BT, L26-P, L26-PBT

**Communication Units**

CPU direct connection (RS-422): All CPU units which support RS-422.
CPU direct connection (USB): QnH CPU units (Q mode) which support USB
CPU direct connection (Ethernet): QnU CPU units which support Ethernet
Remote I/O: AJ72P25/LP25/QLP25, AJ72R25/BR15/QBR15, AJ72T25B, A1SJ72T25B, A1SJ72QBR15/QLP25/QLR25, QJ72LP25G/LP25-25/BR15
Computer link: AJ71C24/UC24, A1SJ71UC24, FX2N-485-BD, FX1N-485-BD, FX2N-232-BD, FX1N-232-BD, FX0N-485ADP, FX2NC-485ADP, FX0N-232ADP, FX2NC-232ADP
Serial communication: AJ71QC24(N), A1SJ71QC24(N), QJ71C24

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CC-Link: AJ65BT-G4, AJ65BT-G4-S3
Ethernet: AJ71E71N, A1SJ71E71N, AJ71E71, A1SJ71E71, AJ71QE71, AJ71QE71N, A1SJ71QE71N, A1SJ71QE71, QJ71E71, QJ71E71-100, QJ71E71-B2, QJ71E71-B5
MELSECNET II: AJ71AP21, A1SJ71AP21
MELSECNET/10: AJ71LP21, AJ71BR11, A1SJ71LP21, A1SJ71BR11
MELSECNET/H: QJ71BR11, QJ71LP21-25, QJ71LP21G, QJ72LP25G, QJ72LP25-25, QJ72BR15
CC-Link IE (formerly MELSECNET/G): QJ71GP21(S)-SX

**Interface Boards for Personal Computers**

MELSECNET/H: Q80BD-J71LP21-25, Q80BD-J71BR11, Q80BD-J71LP21G
CC-Link IE (formerly MELSECNET/G): Q80BD-J71GP21(S)-SX
CC-Link: A80BD-J61BT13, A80BD(E)-J61BT11, Q80BD-J71BR11

## ● Restrictions on CPU Units

• The following CPU Units cannot be used connection test function of EZSocket Builder.
Unsupported models:
Q03UDV, Q04UDV, Q04UDPV, Q06UDV, Q06UDPV, Q13UDV, Q13UDPV, Q26UDV, Q26UDPV, Q50UDEH, Q100UDEH
L02S, L02S-P, L02-P, L06, L06-P, L26, L26-P, L26-PBT

## ● Restrictions on Communication Units

**Serial Communication Units**

• The VDS/ASTMAC system cannot be connected to the RS-422/485 terminals of the computer link or serial communication units since they are controlled by DC voltage.
• For the C24 computer link units, only version S6 or later can be connected.
• With the C24/UC24 computer link units, the VDS/ASTMAC system cannot access devices A/V/Z or extended file register R when the QnA unit is connected. It cannot write to AnSH units (EEPROM operation) when it is running or change the T/C settings.

The C24 units are subject to the following restrictions.

• Even if the AnU unit is installed in the system, only communication equivalent to that of the AnA units is available.
• For units with a model name containing both C24 and UC24, select a communication path according to the software version of a unit connected to them (see user's manuals of respective units for their software versions).
A1SCPU24-R2: UC24 equivalent
A1SJ71C24-PRF: UC24 equivalent for software version of "M" or later
A1SJ71C24-R2: UC24 equivalent for software version of "M" or later
A2CCPU24: UC24 equivalent for software version of "K" or later
A2CCPUC34-PRF: UC24 equivalent for software version of "K" or later

The following list indicates the supported and the unsupported models.

Supported models:
A1SCPUC24-R2, A1SJ71C24-PRF, A1SJ71C24-R2
A1SJ71UC24-PRF, A1SJ71UC24-R2
A2CCPU24, A2CCPU24-PRF
AJ71C24-S6, AJ71C24-S8, AJ71UC24
AJ71UC24-PRF
Unsupported models:
A1SJ71C24-R4, A1SJ71UC24-R4
A2CJ71C24-R4
A1SJ71UC24-R2, A1SJ71UC24-R4-S2
AJ71UC24-S2
AJ71C24, AJ71C24-S3

Use RS-232-C/RS-422 cables recommended by Mitsubishi Electric that are compatible with the serial communication units.

**CPU Units**

Use the following cables for connection to the QnCPU units.

• QC02R4EX (plus conventional RS-422 cable)
• QC30R2

**Ethernet Communication Units**

The following versions or later of Ethernet units (AJ71QE71) for QnA units can be connected.

AJ71QE71, AJ71QE71-B5:
Software version of "C" or later
A1SJ71QE71-B2, A1SJ71QE71-B5:
Software version of "E" or later

The Ethernet units for ACPU (AJ71E71) offer functions equivalent to those of an AnA unit even if they are installed to an AnU unit.

Although a communication error LED is lit for the following versions of Ethernet units for ACPU (AJ71E71) when they are installed to a remote I/O unit, this does not affect their normal operation.

AJ71E71, A1SJ71E71-B2/B5:
Software version of "U" or earlier
AJ71E71-S3, A1SJ71E71-B2-S3/-B5-S3:
Software version of "H" or earlier

**G4 Units (CC-Link)**

The AJ65BT-G4 unit can be connected to the products with the software version of "B" or later. The G4 units on the master unit (AJ61BT11 and AJ61QBT11) can be connected to those with the software version of "N" or later.

## ● Supported MELSEC Devices

### When Accessing to Sequence CPU

| Device | | | | | Applicable CPU | | | | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| Type | | Length | Symbol | Address | Q | QnA | A | FX | L | |
| Special relays | | Bit | SM | Decimal | X | X | | | X | |
| Special registers | | Word | SD | Decimal | X | X | | | X | |
| Input relays | | Bit | X | Hexadecimal | X | X | X | X | X | For FX, the device addresses are in octal format. |
| Output relays | | Bit | Y | Hexadecimal | X | X | X | X | X | |
| Internal relays | | Bit | M | Decimal | X | X | X | X | X | |
| Latch relays | | Bit | L | Decimal | X | X | X | | X | |
| Annunciators | | Bit | F | Decimal | X | X | X | | X | |
| Edge relays | | Bit | V | Decimal | X | X | | | X | |
| Link relays | | Bit | B | Hexadecimal | X | X | X | | X | |
| Data registers | | Word | D | Decimal | X | X | X | | X | |
| Link registers | | Word | W | Hexadecimal | X | X | X | | X | |
| Timers | Contacts | Bit | TS | Decimal | X | X | X | X | X | |
| | Coils | Bit | TC | Decimal | X | X | X | X | X | |
| | Current readings | Word | TN | Decimal | X | X | X | X | X | |
| Counters | Contacts | Bit | CS | Decimal | X | X | X | X | X | |
| | Coils | Bit | CC | Decimal | X | X | X | X | X | |
| | Current readings | Word | CN | Decimal | X | X | X | X | X | |
| Integrating timers | Contacts | Bit | SS | Decimal | | X | | | X | |
| | Coils | Bit | SC | Decimal | | X | | | X | |
| | Current readings | Word | SN | Decimal | | X | | | X | |
| Special link relays | | Bit | SB | Hexadecimal | X | X | X | | X | |
| Special link registers | | Word | SW | Hexadecimal | X | X | X | | X | |
| Step relays | | Bit | S | Decimal | X | X | X | X | X | |
| Direct inputs | | Bit | DX | Hexadecimal | X | X | | | X | |
| Direct outputs | | Bit | DY | Hexadecimal | X | X | | | X | |
| File registers | | Word | R | Decimal | X | X | X | | X | |
| Serial file registers | | Word | ZR | Hexadecimal | X | X | | | X | |
| Extended file registers | | Word | ER | Decimal | | | X | | | |
| Buffer memory | | Word | G | Decimal | X | X | | | X | |

## ● Relationship with Device Tag Objects

| Device Tag Object | | Device Type | | Remarks |
|---|---|---|---|---|
| | | Bit | Word | |
| DI | | X | | |
| DO | | X | | |
| DR | Input | X | | Bit-device output is valid only if device addresses start with a multiple of 16 and the number of access points is a multiple of 16. (*1) |
| | Output | X | | |
| AI | AI input | | X | Access to bit-devices is valid only if device addresses start with a multiple of 16. |
| | BCD input | X | | |
| AO | AO output | | X | |
| | BCD output | X | | |
| AR | | | X | |
| TXT | | | X | Only the data type of “UI2” and the character code of “ShiftJIS” can be used. |
| XAI | | | X | |
| XAO | | | X | |
| XAR | | | X | |
| XTX | | | | |
| BD | I/O address | | X | |
| | I/O address for start-reading check (read) | | X | Specify data in ASCII. |
| | I/O address for end-reading notification (read) | | X | |
| | Write-permission register (write) | | X | |
| | I/O address for end-writing notification (write) | | X | |

*1: Using Cv to batch-write array elements of DR, these restrictions are valid (the addresses must start with a multiple of 16 and the number of access points must be a multiple of 16). However, using Cvi(n) to write each array element of DR, neither of them are valid (the addresses can start with a non-multiple of 16 and the number of access points can be a non-multiple of 16).

## ■ ASYNCHRONOUS TYPE

### ● Interface Specifications

**Communication Interface**

Ethernet:
Method of access to device data:
Continuous bit access
Continuous word access
Asynchronous event reception (on-demand processing):
Received text: 128 bytes max.
RS-232-C:
Method of access to device data:
Continuous bit access
Continuous word access

### ● Applicable Models

- A series
- QnA series
- Q series (*1) (*2)

*1: Only the devices covered by the A series can be accessed. Devices Ms and Ds between 9000 to 9999 cannot be accessed.
*2: The universal model (QnU) CPU unit is required to support A compatible 1E frame or A compatible 1C frame.

### ● Communication Protocol Specifications

**Ethernet Driver**

Communication protocol:
Interface: Ethernet
Supported model:
Mitsubishi Electric:
AJ71E71 Ethernet interface unit (version K or later)
QE71 Ethernet interface unit (*1)
QJ71E71 Ethernet interface unit (*1)
Communication function:
Access to data in sequencer CPU
Reception of sequencer asynchronous event
Data format: ASCII
Protocol: UDP/IP
Port No.: Specifiable
VDS: Specifiable.
MELSEC: Specifiable by MELSEC.
Update method:
Reading/writing data from/to sequence CPU
Through fixed buffer

Note: Specify the IP address or node name at the other end of the line. ACPU monitoring timers 0 to 9 are available (*1) (250 ms).

*1: Operates within the A compatible 1E frame.

**RS-232-C Driver**

Communication protocol:
Interface: RS-232-C
Supported model:
Mitsubishi Electric:
AJ71C24-S8 Computer link unit
AJ71UC24 Computer link unit (*1)
A0J2-C214S1 Computer link unit (*1)
AJ71QC24 Computer link unit (*1)
Protocol: A compatible 1C frame (control procedure 4 only)
Transmission method: Half-duplex
Synchronization method: Start-stop synchronization
Transmission speed: 300, 600, 1200, 2400, 4800, 9600, 19200 bps
Data format:
Start bit: 1
Data bit: 7 or 8
Parity bit: 0: none; 1: odd; 2: even
Sum check: Yes/no
Specification of terminator character:
Available for control procedure 4
Transmission wait: 0 to 15 (x 10) msec

Note: Specify the COM port number used.

*1: Operates the function covered by the AJ71C24-S8 computer link unit.

### ● Supported Devices

The following table shows the devices that can be handled with the MELSEC I/O driver contained in this driver software package.

**Bit device**

Input relays: X
Output relays: Y
Internal relays: M
Special relays: M
Latch relays: L
Step relays: S
Link relays: B

**Word devices**

Data registers: D
Special registers: D
Link registers: W
File registers (*1): R

*1: The extended file registers are not supported. This device can be used only by A series.

### ● Relationship to Device Tag Objects

The following table shows the relationship between the device types acquired by the MELSEC I/O driver contained in this driver software package and the device tag objects.

| Device Tag Object Type | | Specifiable Device Types | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Bit Device | | | | | | Word Device | | | Asynchronous Data |
| | | X | Y | M | L | S | B | D | W | R | ONDEMAND |
| DI | | X | | X | X | X | X | | | | |
| DO | | | X | X | X | X | X | | | | |
| DR | Input | X | | X | X | X | X | | | | |
| | Input/output | | X | X | X | X | X | | | | |
| AI (*1) | AI input | X | | X | X | X | X | X | X | X | |
| | BCD | X | | X | X | X | X | | | | |
| AO (*1) | AO output | | X | X | X | X | X | X | X | X | |
| | BCD | | X | X | X | X | X | | | | |
| AR | | | | | | | | X | X | X | |
| TXT | | | | | | | | X | X | X | X |
| XAI | | | | | | | | X | X | X | |
| XAO | | | | | | | | X | X | X | |
| XAR | | | | | | | | X | X | X | |
| XTX | | | | | | | | | | | |
| BD (*1) | Input trigger | X | | X | X | X | X | X | X | X | X |
| | Input data | X | | X | X | X | X | X | X | X | |
| | Output data | | X | X | X | X | X | X | X | X | |
| | Notification of input/output completion | | X | X | X | X | X | X | X | X | |
| | Output permission | X | | X | X | X | X | X | X | X | |

X: Indicates that the device type can be specified with the corresponding object type.

*1: When a bit device is specified, the data is handled as 16-bit data.

## ■ MODEL AND SUFFIX CODE

| Model | Suffix Code | Description |
|---|---|---|
| NT351AJ | -LW11A | MELSEC Driver |

## ■ ORDERING INFORMATION

Specify the model and suffix codes.

## ■ RELATED DOCUMENT

• VDS, GS 34P02A02-01E

## ■ TRADEMARKS

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