

# General Specifications

## TI-544-01

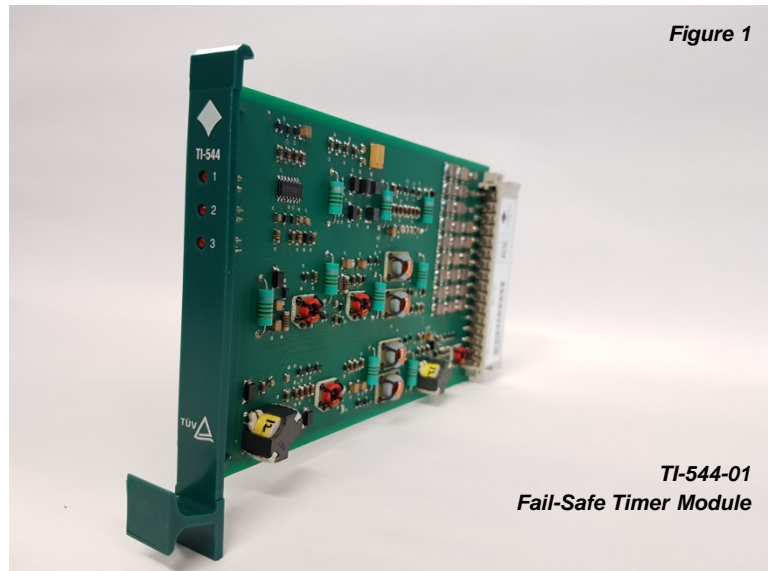
ProSafe-SLS™

GS48C44Z01-00E-N

Fail-Safe Timer Module

### ■ GENERAL

This module contains a single channel fail-safe delay-off Timer circuit.

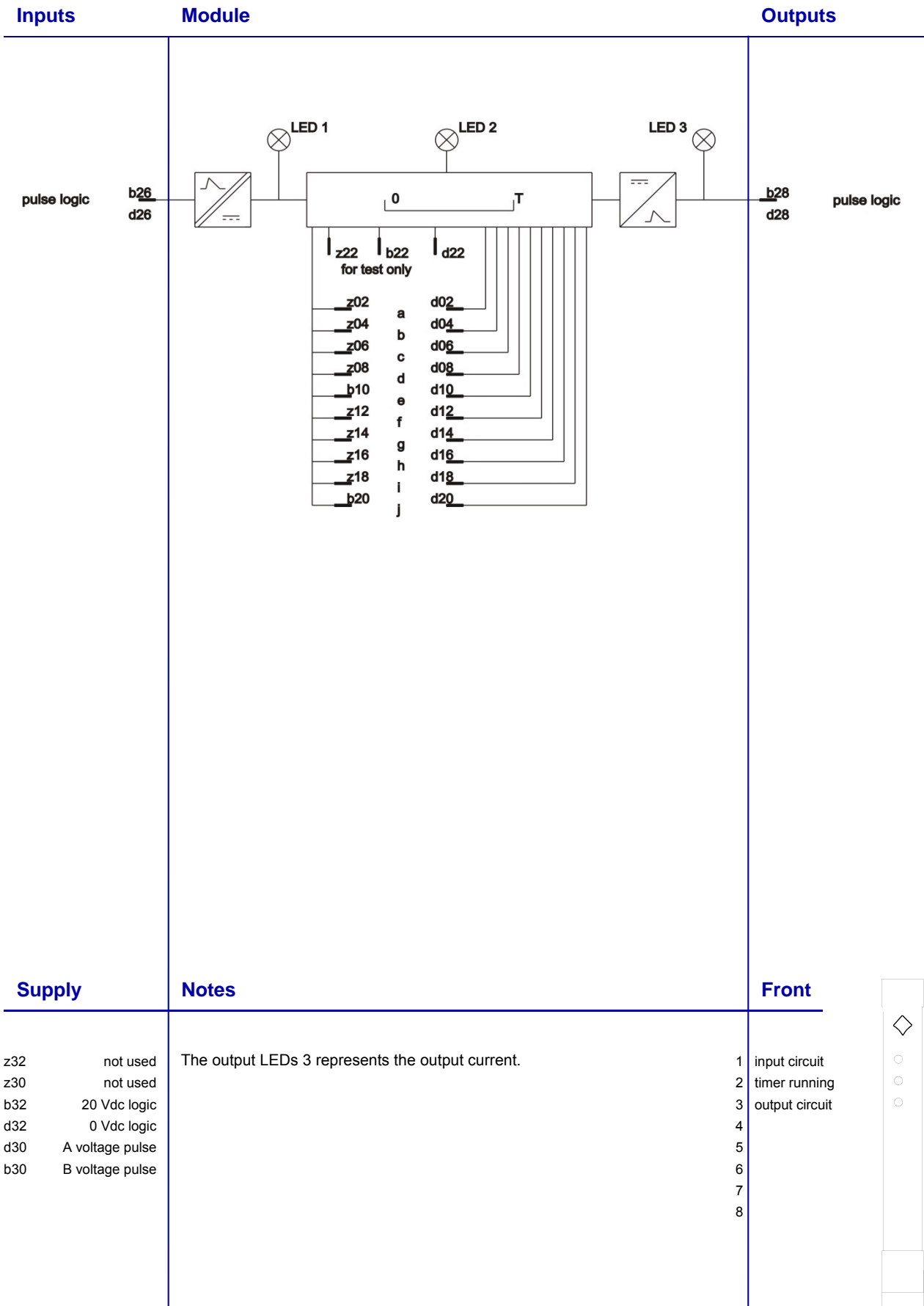


Timer setting is done by connector strapping. The timer is suitable for a timer range of 1.5 – 310 sec. The delay function is based on the controlled discharge of a capacitor.

The input signal is used to generate a pulse of approximately 1 second which fully charges the capacitor(s).

Depending on the time strapping, one or more capacitors are used. As long as the input signal is present, the capacitors remain charged. When the input signal is removed, the capacitors discharge over a resistor network. When the capacitors are discharged, the output will no longer generate pulses. The module is provided with 3 LEDs indicating: input, output and running of the timer.

FUNCTIONAL DIAGRAM



## ■ SPECIFICATIONS

Description		Data
General	Number of channels	1
	Width	3HP
	Identification	TI-544 on front and more detailed on connector label
	Weight	135 gram
Input	Pulse Logic Unit Load Status indication Minimum trigger time	Current pulses 500 mA 1 Red LED 1 msec.
Output	Output type Capacity Status indication	Current pulses 500 mA 10 unit loads Red LED
	Running indication	Red LED (blinking)
	Timing errors: Capacitor Tolerance Circuit tolerance Temperature tolerance	10% 5% 7% (full range)
Propagation	On delay	4 - 10 ms
Supply	Logic supply	20 Vdc 15 mA
	Clock	A and B pulse, level 0 / 20 V
Dissipation		< 0.3 W

■ Time Strapping

Connections

a: z02 - d02  
 b: z04 - d04  
 c: z06 - d06  
 d: z08 - d08  
 e: b10 - d10  
 f: z12 - d12  
 g: z14 - d14  
 h: z16 - d16  
 i: z18 - d18  
 j: b20 - d20

Time settings

seconds  
 1.5  
 3 a  
 4.5 b  
 6 ab  
 7.5 d  
 9 a d  
 10 b d  
 12 ab d  
 15 a f  
 20 d f  
 25 ab d f  
 30 g  
 35 ab g  
 40 b d g  
 45 a fg  
 50 a d fg  
 55 defg  
 60 bcdefg  
 70 abc h  
 80 ab f h  
 90 b def h  
 100 a d gh  
 110 d fgh  
 120 b defgh  
 130 bc j  
 140 b f j  
 150 a def j  
 160 d g j  
 170 ab fg j  
 180 a defg j  
 190 ab h j  
 200 a f h j  
 220 ab gh j  
 240 defgh j  
 260 f hij  
 280 b ghij  
 300 bcd fghij  
 310 abcdefghij