Failure Modes, Effects and Diagnostic Analysis

Project:
TDLS200 Tunable Diode Laser Analyzer

Company:
Yokogawa Electric Corporation
Tokyo
Japan

Contract Number: Q10/01-01
Report No.: YEC 10/01-01 R001
Version V1, Revision R2, March 26, 2010
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Management Summary

This report summarizes the results of the hardware assessment in the form of a Failure Modes, Effects, and Diagnostic Analysis (FMEDA) of the TDLS200 Tunable Diode Laser Analyzer. A Failure Modes, Effects, and Diagnostic Analysis is one of the steps to be taken to achieve functional safety certification per IEC 61508 of a device. From the FMEDA, failure rates and Safe Failure Fraction are determined. The FMEDA that is described in this report concerns only the hardware of the TDLS 200. Only the 4-20mA output was analyzed for this report; no other outputs were considered. For full functional safety certification purposes all requirements of IEC 61508 must be considered.

The TDLS200 TDL analyzer is designed to measure selected target gases in gas phase samples directly at the process point, close coupled/by-pass leg or in full extractive systems (flow cell). The analyzer measures free molecules on a path averaged basis.

The basic TDLS200 analyzer comprises two units, the Launch Control Unit and Detect Unit. Various Process Interface configurations are available for connecting the analyzer to the measurement point.

The TDLS 200 is classified as a Type B[1] device according to IEC 61508, having a hardware fault tolerance of 0. The analysis shows that the device has a Safe Failure Fraction between 60% and 90% (assuming that the logic solver is programmed to detect under-scale currents) and therefore meets hardware architectural constraints for up to SIL 1 as a single device.

The failure rates for the TDLS 200 are listed in Table 1.

Table 1 Failure rates TDLS 200

Failure Category	Failure Rate (FIT)
Fail Safe Undetected	1198
Fail Dangerous Detected	10595
Fail Dangerous Undetected	2401
Residual	2690

These failure rates are valid for the useful lifetime of the product, see Appendix A.

The failure rates listed in this report do not include failures due to wear-out of any components. They reflect random failures and include failures due to external events, such as unexpected use, see section 4.2.2.

[1] Type B device: “Complex” component (using micro controllers or programmable logic); for details see 7.4.3.1.3 of IEC 61508-2.

Table 2 lists the failure rates for the TDLS 200 according to IEC 61508.

Table 2 Failure rates according to IEC 61508

Device	λ_{SD}	λ_{SU}[2]	λ_{DD}	λ_{DU}	SFF[3]
TDLS 200	0 FIT	3888 FIT	10595 FIT	2401 FIT	85.8%

A user of the TDLS 200 can utilize these failure rates in a probabilistic model of a safety instrumented function (SIF) to determine suitability in part for safety instrumented system (SIS) usage in a particular safety integrity level (SIL). A full table of failure rates is presented in section 4.4 along with all assumptions.

[2] It is important to realize that the Residual failures are included in the Safe Undetected failure category according to IEC 61508. Note that these failures on their own will not affect system reliability or safety, and should not be included in spurious trip calculations

[3] Safe Failure Fraction needs to be calculated on (sub)system level

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1 Purpose and Scope

Generally three options exist when doing an assessment of sensors, interfaces and/or final elements.

Option 1: Hardware assessment according to IEC 61508

Option 1 is a hardware assessment by *exida* according to the relevant functional safety standard(s) like IEC 61508 or EN 954-1. The hardware assessment consists of a FMEDA to determine the fault behavior and the failure rates of the device, which are then used to calculate the Safe Failure Fraction (SFF) and the average Probability of Failure on Demand (PFD_{AVG}). When appropriate, fault injection testing will be used to confirm the effectiveness of any self-diagnostics.

This option provides the safety instrumentation engineer with the required failure data as per IEC 61508 / IEC 61511. This option does not include an assessment of the development process.

Option 2: Hardware assessment with proven-in-use consideration per IEC 61508 / IEC 61511

Option 2 extends Option 1 with an assessment of the proven-in-use documentation of the device including the modification process.

This option for pre-existing programmable electronic devices provides the safety instrumentation engineer with the required failure data as per IEC 61508 / IEC 61511. When combined with plant specific proven-in-use records, it may help with prior-use justification per IEC 61511 for sensors, final elements and other PE field devices.

Option 3: Full assessment according to IEC 61508

Option 3 is a full assessment by *exida* according to the relevant application standard(s) like IEC 61511 or EN 298 and the necessary functional safety standard(s) like IEC 61508 or EN 954-1. The full assessment extends Option 1 by an assessment of all fault avoidance and fault control measures during hardware and software development.

This option provides the safety instrumentation engineer with the required failure data as per IEC 61508 / IEC 61511 and confidence that sufficient attention has been given to systematic failures during the development process of the device.

This assessment shall be done according to option 1.

This document shall describe the results of the hardware assessment in the form of the Failure Modes, Effects and Diagnostic Analysis carried out on the TDLS 200. From this, failure rates, Safe Failure Fraction (SFF) and example PFD_{AVG} values are calculated.

The information in this report can be used to evaluate whether a sensor subsystem meets the average Probability of Failure on Demand (PFD_{AVG}) requirements and the architectural constraints / minimum hardware fault tolerance requirements per IEC 61508 / IEC 61511.

2 Project Management

2.1 *exida*

exida is one of the world's leading knowledge companies specializing in automation system safety and availability with over 300 years of cumulative experience in functional safety. Founded by several of the world's top reliability and safety experts from assessment organizations and manufacturers, *exida* is a partnership with offices around the world. *exida* offers training, coaching, project oriented consulting services, safety lifecycle engineering tools, detailed product assurance and certification analysis and a collection of on-line safety and reliability resources. *exida* maintains a comprehensive failure rate and failure mode database on process equipment.

2.2 Roles of the parties involved

Yokogawa Electric Corporation	Manufacturer of the TDLS 200
exida	Performed the hardware assessment according to Option 1 (see Section 1)

exida was contracted in June 2009 with the hardware assessment of the above-mentioned device.

2.3 Standards and Literature used

The services delivered by *exida* were performed based on the following standards / literature.

[N1]	IEC 61508-2: 2000	Functional Safety of Electrical/Electronic/Programmable Electronic Safety-Related Systems
[N2]	Electrical & Mechanical Component Reliability Handbook, 2nd Edition, 2008	exida L.L.C, Electrical & Mechanical Component Reliability Handbook, Second Edition, 2008, ISBN 978-0-9727234-6-6
[N3]	Safety Equipment Reliability Handbook, 3rd Edition, 2007	exida L.L.C, Safety Equipment Reliability Handbook, Third Edition, 2007, ISBN 978-0-9727234-9-7
[N4]	Goble, W.M. 1998	Control Systems Safety Evaluation and Reliability, ISA, ISBN 1-55617-636-8. Reference on FMEDA methods
[N5]	IEC 60654-1:1993-02, second edition	Industrial-process measurement and control equipment – Operating conditions – Part 1: Climatic condition
[N6]	Goble, W.M. and Cheddie, H., 2005	Safety Instrumented Systems Verification, Practical Probabilistic Calculations, ISA, ISBN 1-55617-909-X

2.4 Reference documents

2.4.1 Documentation provided by Yokogawa

[D1]	Bulletin 11Y01B01-51E, Ed:01/b, 2009	Data Sheet, TDLS200 TruePeak Tunable Diode Laser Spectrometer
[D2]	TDLS200 Instruction Manual, V2.1	Instruction Manual / Safety Manual
[D3]	Doc # 2000-2010, Rev C, April 20, 2005	TDLS Analyzer Electronic Block Diagram (contains proprietary information)
[D4]	Doc # 2000-1040, Rev C, April 16, 2008	Schematic, Back Plane Board (contains proprietary information)
[D5]	(unnumbered document), Rev X2, October 9, 2004	Schematic, FPGA Board (contains proprietary information)
[D6]	Doc # 2000-1024, Rev A, November 23, 2005	Schematic, Analog Input and Output Board (contains proprietary information)
[D7]	Doc # 2000-1023, Rev B, October 5, 2005	Schematic, O2 Det/Power Board (contains proprietary information)
[D8]	TDLS200 Electrolytic Report Dec 17 2009.pdf	Electrolytic Capacitor Impact Analysis Report
[D9]	TDLS200 Electrolytic Capacitor Test.pdf, March 19, 2010	Fault Injection Test Report, TDLS200

2.4.2 Documentation generated by *exida*

[R1]	TDLS200 Analog IO Board.efm, October 26, 2009	Failure Modes, Effects, and Diagnostic Analysis – TDLS 200, Analog Input and Output Board (contains proprietary information)
[R2]	TDLS200 Backplane Board.efm, October 26, 2009	Failure Modes, Effects, and Diagnostic Analysis – TDLS 200, Back Plane Board (contains proprietary information)
[R3]	TDLS200 Detector Board.efm, October 26, 2009	Failure Modes, Effects, and Diagnostic Analysis – TDLS 200, O2 Det/Power Board (contains proprietary information)
[R4]	TDLS200 FPGA Board.efm, October 23, 2009	Failure Modes, Effects, and Diagnostic Analysis – TDLS 200, FPGA Board (contains proprietary information)
[R5]	TDLS200 Summary.xls, October 26, 2009	Failure Modes, Effects, and Diagnostic Analysis - Summary –TDLS 200 (contains proprietary information)
[R6]	YEC 10-01-01 R001 V1 R2 TDLS200 FMEDA.doc,	FMEDA report, TDLS 200 (this report)

	03/26/2010	

3 Product Description

The TDLS200 TDL analyzer is designed to measure selected target gases in gas phase samples directly at the process point, close coupled/by-pass leg or in full extractive systems (flow cell). The analyzer measures free molecules on a path averaged basis. Measurements are possible (with correct analyzer configuration) at the following conditions:

- Gas temperatures up to 1500°C (2730°F)
- Gas pressures up to 10 BarG (145 psig)
- High Particulate Loading (as a function of measurement path length)

The standard analyzer is designed for operation in a Safe Area (General Purpose). The addition of a Purge System facilitates operation in Hazardous Areas.

The basic TDLS200 analyzer comprises two units, the Launch Control Unit and Detect Unit. Various Process Interface configurations are available for connecting the analyzer to the measurement point. Several options may be added to the standard analyzer such as:

- Analog I/O board
- Mini Display
- 6.5” screen and keypad
- Display sun shield
- Optional Universal Power Supply (with or without a Mini Display)
- Remote Interface Unit (not required for normal operation)
- Hazardous Area purge systems

Figure 1 shows a block diagram of the TDLS 200. Referring to this diagram, the FMEDA covers the Oxygen Detector Circuit Board, FPGA Board, Analog I/O Board power supply and output, and Single Board Computer (SBC). The FMEDA covers the Backplane Board including the board temperature, DC power distribution, on/off switch, resettable thermal fuse, and watchdog timer sections. The FMEDA also covers the laser, detector, and Peltier module.

The FMEDA does NOT cover the Backplane Board USB ports, RJ-45, alarm relays, and valve relays. The FMEDA does NOT cover the Analog I/O Board auxiliary inputs, Display Interface Board, the TFT display, the Key Pad, the Mini Display, the external power supply, or the hazardous area purge systems.

The TDLS 200 is classified as a Type B[4] device according to IEC 61508, having a hardware fault tolerance of 0.

[4] Type A device: “Non-Complex” subsystem (using discrete elements); for details see 7.4.3.1.2 of IEC 61508-2./ Type B device: “Complex” component (using micro controllers or programmable logic); for details see 7.4.3.1.3 of IEC 61508-2.

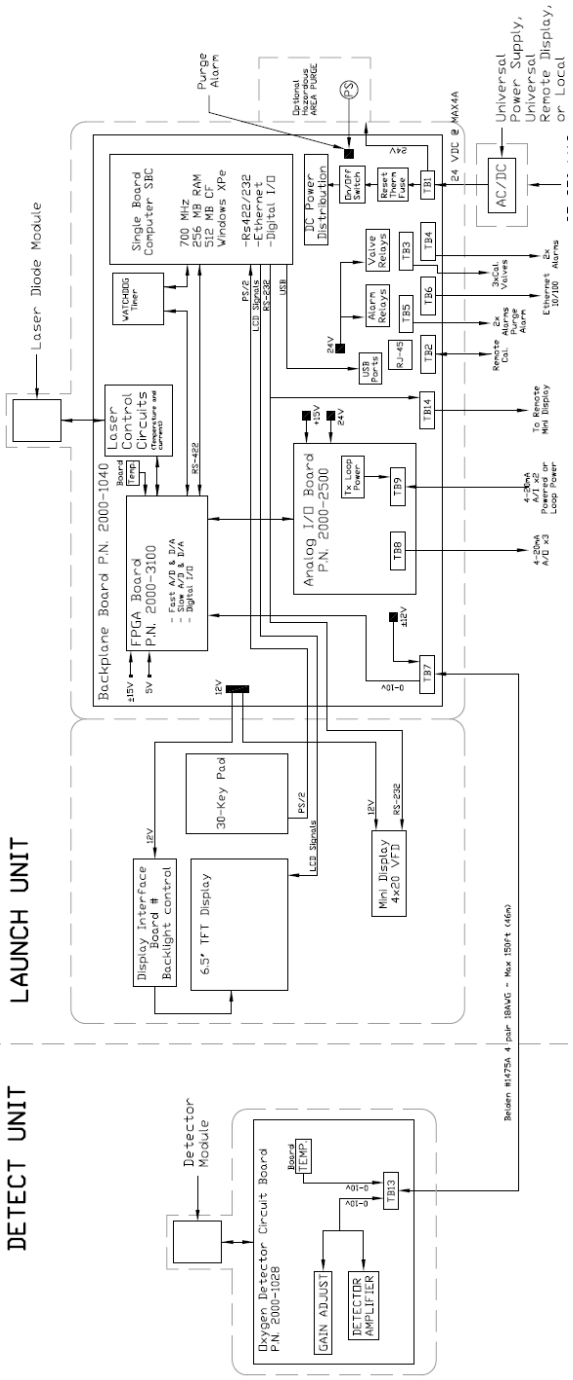

Figure 1 TDLS 200, Parts included in the FMEDA

4 Failure Modes, Effects, and Diagnostic Analysis

The Failure Modes, Effects, and Diagnostic Analysis was performed based on the documentation obtained from Yokogawa and is documented in [R1] - [R5].

When the effect of a certain failure mode could not be analyzed theoretically, the failure modes were introduced at the component level and the effects of these failure modes were examined on system level, See Fault Injection Test Report [D6].

4.1 Failure Categories description

In order to judge the failure behavior of the TDLS 200, the following definitions for the failure of the device were considered.

Fail-Safe State	State where the output exceeds the user defined threshold
Fail Safe	Failure that causes the device to go to the defined fail-safe state without a demand from the process.
Fail Detected	Failure that causes the output signal to go to the predefined alarm state (<3.9 mA).
Fail Dangerous	Failure that deviates the measured input state or the actual output by more than 2% of span and that leaves the output within active scale
Fail Dangerous Undetected	Failure that is dangerous and that is not being diagnosed by automatic diagnostics
Fail Dangerous Detected	Failure that is dangerous but is detected by automatic diagnostics
Residual	Failure of a component that is part of the safety function but that has no effect on the safety function.

The failure categories listed above expand on the categories listed in IEC 61508 which are only safe and dangerous, both detected and undetected. In IEC 61508, Edition 2000, the Residual failures are defined as safe undetected failures even though they will not cause the safety function to go to a safe state. Therefore they need to be considered in the Safe Failure Fraction calculation.

4.2 Methodology – FMEDA, Failure Rates

4.2.1 FMEDA

A Failure Modes and Effects Analysis (FMEA) is a systematic way to identify and evaluate the effects of different component failure modes, to determine what could eliminate or reduce the chance of failure, and to document the system in consideration.

A FMEDA (Failure Mode Effect and Diagnostic Analysis) is an FMEA extension. It combines standard FMEA techniques with the extension to identify online diagnostics techniques and the failure modes relevant to safety instrumented system design. It is a technique recommended to generate failure rates for each important category (safe detected, safe undetected, dangerous detected, dangerous undetected, fail high, fail low, etc.) in the safety models. The format for the FMEDA is an extension of the standard FMEA format from MIL STD 1629A, Failure Modes and Effects Analysis.

4.2.2 Failure Rates

The failure rate data used by *exida* in this FMEDA is from the Electrical and Mechanical Component Reliability Handbook which was derived using field failure data from multiple sources and failure data from various databases. The rates were chosen in a way that is appropriate for safety integrity level verification calculations. The rates were chosen to match exida Profile 3, see Table 3. It is expected that the actual number of field failures due to random events will be less than the number predicted by these failure rates.

Table 3 exida Environmental Profiles

EXIDA ENVIRONMENTAL PROFILE		GENERAL DESCRIPTION	PROFILE PER IEC 60654-1	AMBIENT TEMPERATURE [°C]		TEMP CYCLE [°C / 365 DAYS]
				AVERAGE (EXTERNAL)	MEAN (INSIDE BOX)	
1	Cabinet Mounted Equipment	Cabinet mounted equipment typically has significant temperature rise due to power dissipation but is subjected to only minimal daily temperature swings	B2	30	60	5
2	Low Power /Mechanical Field Products	Mechanical / low power electrical (two-wire) field products have minimal self heating and are subjected to daily temperature swings	C3	25	30	25
3	General Field Equipment	General (four-wire) field products may have moderate self heating and are subjected to daily temperature swings	C3	25	45	25
4	Unprotected Mechanical Field Products	Unprotected mechanical field products with minimal self heating, are subject to daily temperature swings and rain or condensation.	D1	25	30	35

For hardware assessment according to IEC 61508 only random equipment failures are of interest. It is assumed that the equipment has been properly selected for the application and is adequately commissioned such that early life failures (infant mortality) may be excluded from the analysis.

Failures caused by external events however should be considered as random failures. Examples of such failures are loss of power, physical abuse, or problems due to intermittent instrument air quality.

The assumption is also made that the equipment is maintained per the requirements of IEC 61508 or IEC 61511 and therefore a preventative maintenance program is in place to replace equipment before the end of its “useful life”. Corrosion, erosion, coil burnout etc. are considered age related (late life) or systematic failures, provided that materials and technologies applied are indeed suitable for the application, in all modes of operation.

The user of these numbers is responsible for determining their applicability to any particular environment. Accurate plant specific data may be used for this purpose. If a user has data collected from a good proof test reporting system that indicates higher failure rates, the higher numbers shall be used. Some industrial plant sites have high levels of stress. Under those conditions the failure rate data is adjusted to a higher value to account for the specific conditions of the plant.

4.3 Assumptions

The following assumptions have been made during the Failure Modes, Effects, and Diagnostic Analysis of the TDLS 200.

- Only a single component failure will fail the entire TDLS 200
- Failure rates are constant, wear-out mechanisms are not included
- Propagation of failures is not relevant
- All components that are not part of the safety function and cannot influence the safety function (feedback immune) are excluded
- The stress levels are average for an industrial environment and can be compared to exida Profile 3 with temperature limits within the manufacturer's rating. Other environmental characteristics are assumed to be within manufacturer's rating.
- The TDLS 200 is configured so that all fault and warning conditions result in the output going to the 3.3mA block state.
- The Ethernet and serial links are only used for setup, calibration, and diagnostic purposes, not for safety critical operation.
- The application program in the logic solver is constructed in such a way that Fail Low failures are detected regardless of the effect, safe or dangerous, on the safety function.
- Materials are compatible with process conditions
- The device is installed per manufacturer's instructions
- External power supply failure rates are not included
- Worst-case internal fault detection time is less than one hour.

4.4 Results

Using reliability data extracted from the *exida* Electrical and Mechanical Component Reliability Handbook the following failure rates resulted from the TDLS 200 FMEDA.

Table 4 Failure rates TDLS 200

Failure Category	Failure Rate (FIT)
Fail Safe Undetected	1198
Fail Dangerous Detected	10595
Fail Dangerous Undetected	2401
Residual	2690

These failure rates are valid for the useful lifetime of the product, see Appendix A.

Table 5 lists the failure rates for the TDLS 200 according to IEC 61508. According to IEC 61508 [N1], the Safe Failure Fraction of a subsystem should be determined.

However as the TDLS 200 is only one part of a subsystem, the SFF should be calculated for the entire sensor / logic / final element combination. The Safe Failure Fraction is the fraction of the overall failure rate of a device that results in either a safe fault or a diagnosed unsafe fault. This is reflected in the following formulas for SFF: SFF = 1 - $\lambda_{DU} / \lambda_{TOTAL}$

Table 5 Failure rates according to IEC 61508

Device	λ_{SD}	λ_{SU}[5]	λ_{DD}	λ_{DU}	SFF[6]
TDLS 200	0 FIT	3888 FIT	10595 FIT	2401 FIT	85.8%

The architectural constraint type for the TDLS 200 is B. The hardware fault tolerance of the device is 0. The SFF and required SIL determine the level of hardware fault tolerance that is required per requirements of IEC 61508 [N1] or IEC 61511. The SIS designer is responsible for meeting other requirements of applicable standards for any given SIL as well.

[5] It is important to realize that the Residual failures are included in the Safe Undetected failure category according to IEC 61508. Note that these failures on their own will not affect system reliability or safety, and should not be included in spurious trip calculations

[6] Safe Failure Fraction needs to be calculated on (sub)system level

5 Using the FMEDA Results

The following section(s) describe how to apply the results of the FMEDA.

5.1 PFD_{AVG} Calculation TDLS 200

An average Probability of Failure on Demand (PFD_{AVG}) calculation is performed for a single (1oo1) TDLS 200. The failure rate data used in this calculation are displayed in section 4.4. A mission time of 10 years has been assumed and a Mean Time To Restoration of 24 hours. For the proof tests a proof test coverage of 90% has been assumed, see Appendix B.

The resulting PFD_{AVG} values for a variety of proof test intervals are displayed in Figure 2. As shown in the graph the PFD_{AVG} value for a single TDLS 200, with a proof test interval of 1 year equals 2.02E-02.

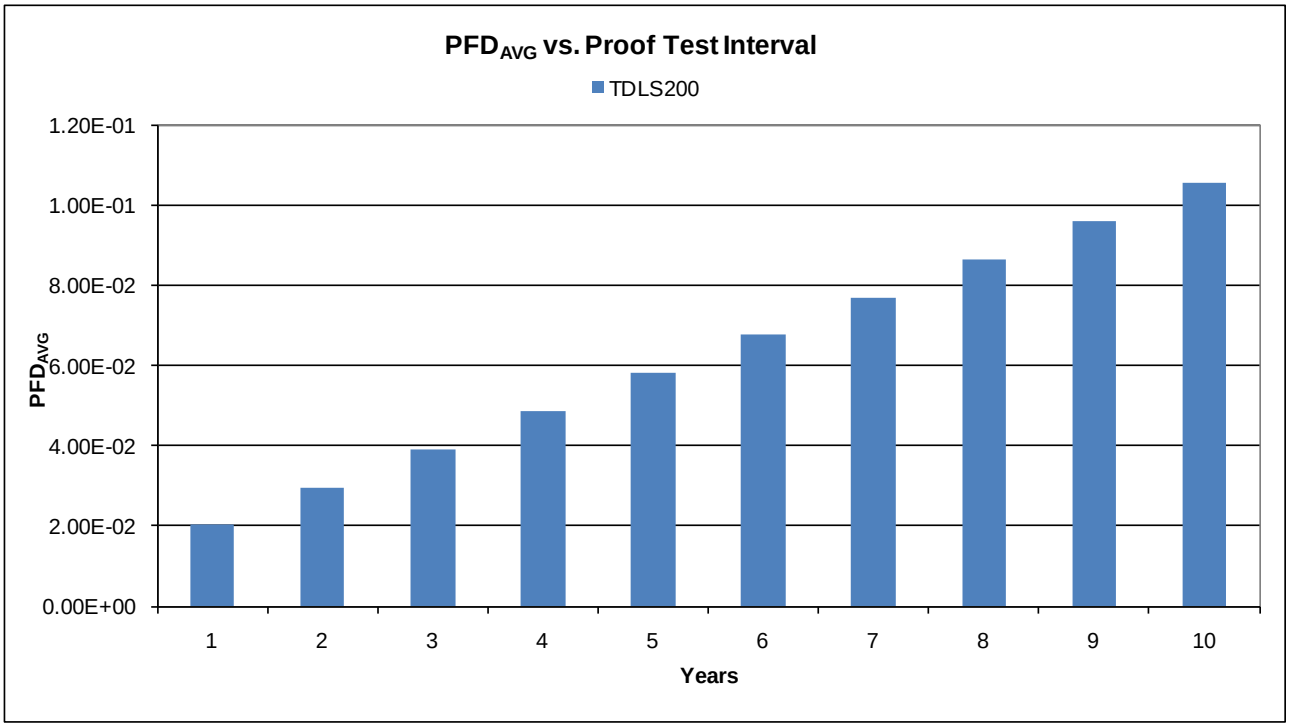

Figure 2: PFD_{AVG} vs. Proof Test Interval

It is the responsibility of the Safety Instrumented Function designer to do calculations for the entire SIF. *exida* recommends the accurate Markov based exSILentia tool for this purpose.

For SIL 1 applications, the PFD_{AVG} value needs to be $\geq 10^{-2}$ and $< 10^{-1}$. This means that for a SIL 1 application, the PFD_{AVG} for a 1-year Proof Test Interval of the TDLS 200 is approximately equal to 20% of the range.

These results must be considered in combination with PFD_{AVG} values of other devices of a Safety Instrumented Function (SIF) in order to determine suitability for a specific Safety Integrity Level (SIL).

6 Terms and Definitions

FIT	Failure In Time (1x10-9 failures per hour)
FMEDA	Failure Mode Effect and Diagnostic Analysis
HFT	Hardware Fault Tolerance
Low demand mode	Mode, where the frequency of demands for operation made on a safety-related system is no greater than twice the proof test frequency.
PFD_{AVG}	Average Probability of Failure on Demand
SFF	Safe Failure Fraction, summarizes the fraction of failures, which lead to a safe state and the fraction of failures which will be detected by diagnostic measures and lead to a defined safety action.
SIF	Safety Instrumented Function
SIL	Safety Integrity Level
SIS	Safety Instrumented System – Implementation of one or more Safety Instrumented Functions. A SIS is composed of any combination of sensor(s), logic solver(s), and final element(s).
Type A component	“Non-Complex” component (using discrete elements); for details see 7.4.3.1.2 of IEC 61508-2
Type B component	“Complex” component (using micro controllers or programmable logic); for details see 7.4.3.1.3 of IEC 61508-2

7 Status of the Document

7.1 Liability

exida prepares FMEDA reports based on methods advocated in International standards. Failure rates are obtained from a collection of industrial databases. *exida* accepts no liability whatsoever for the use of these numbers or for the correctness of the standards on which the general calculation methods are based.

Due to future potential changes in the standards, best available information and best practices, the current FMEDA results presented in this report may not be fully consistent with results that would be presented for the identical product at some future time. As a leader in the functional safety market place, *exida* is actively involved in evolving best practices prior to official release of updated standards so that our reports effectively anticipate any known changes. In addition, most changes are anticipated to be incremental in nature and results reported within the previous three year period should be sufficient for current usage without significant question.

Most products also tend to undergo incremental changes over time. If an *exida* FMEDA has not been updated within the last three years and the exact results are critical to the SIL verification you may wish to contact the product vendor to verify the current validity of the results.

7.2 Releases

Version:	V1	
Revision:	R2	
Version History:	V1, R2	Updated per results of fault injection, March 26, 2010
	V1, R1:	Released to Yokogawa Electric Corporation; March 8, 2010
V0, R1:	Internal draft; March 5, 2010	
	Author(s):	R. Chalupa
Review:	V0, R1:	Rachel Amkreutz (exida); March 7, 2010
Release Status:	Released to Yokogawa Electric Corporation	

7.3 Future Enhancements

At request of client.

7.4 Release Signatures

Chris O'Brien, Director of Business Development

Rudolf P. Chalupa, Senior Safety Engineer

Appendix A Lifetime of Critical Components

According to section 7.4.7.4 of IEC 61508-2, a useful lifetime, based on experience, should be assumed.

Although a constant failure rate is assumed by the probabilistic estimation method (see section 4.2.2) this only applies provided that the useful lifetime[7] of components is not exceeded. Beyond their useful lifetime the result of the probabilistic calculation method is therefore meaningless, as the probability of failure significantly increases with time. The useful lifetime is highly dependent on the subsystem itself and its operating conditions.

This assumption of a constant failure rate is based on the bathtub curve. Therefore it is obvious that the PFD_{AVG} calculation is only valid for components that have this constant domain and that the validity of the calculation is limited to the useful lifetime of each component.

Table 17 shows which components are contributing to the dangerous undetected failure rate and therefore to the PFD_{AVG} calculation and what their estimated useful lifetime is.

Table 6 Useful lifetime of components contributing to dangerous undetected failure rate

Component	Useful Life
Capacitor (electrolytic) - Tantalum electrolytic, solid electrolyte	Approx. 500,000 hours

It is the responsibility of the end user to maintain and operate the TDLS 200 per manufacturer's instructions. Furthermore regular inspection should show that all components are clean and free from damage.

The limiting factors with regard to the useful lifetime of the system are the Tantalum electrolytic capacitors. The Tantalum electrolytic capacitors have an estimated useful lifetime of about 50 years. Note that while the aluminum electrolytic apacitors have a shorter lifetime (approx. 90,000 hours), fault injection testing confirmed that the loss of these components (the most common failure mode) did not affect the operation of the TDLS 200.

When plant experience indicates a shorter useful lifetime than indicated in this appendix, the number based on plant experience should be used.

[7] Useful lifetime is a reliability engineering term that describes the operational time interval where the failure rate of a device is relatively constant. It is not a term which covers product obsolescence, warranty, or other commercial issues.

Appendix B Proof tests to reveal dangerous undetected faults

According to section 7.4.3.2.2 f) of IEC 61508-2 proof tests shall be undertaken to reveal dangerous faults which are undetected by diagnostic tests. This means that it is necessary to specify how dangerous undetected faults which have been noted during the Failure Modes, Effects, and Diagnostic Analysis can be detected during proof testing.

B.1 Suggested Proof Test

A suggested proof test is listed in Table 7. This test will detect > 90% of possible DU failures in the device.

Table 7 Suggested Proof Test

Step	Action
1.	Bypass the safety function and take appropriate action to avoid a false trip
2.	Use digital communications to retrieve any diagnostics and take appropriate action.
3.	Send a digital command to the transmitter to go to the block state current output and verify that the analog current reaches that value[8].
4.	Perform a two-point calibration[9] of the analyzer over the full working range.
5.	Remove the bypass and otherwise restore normal operation

[8] This tests for possible quiescent current related failures.

[9] If the two-point calibration is performed with electrical instrumentation, this proof test will not detect any failures of the sensor